NOVEL III-V DEVICE ARCHITECTURES

FOR APPLICATION IN ADVANCE

CMOS LOGIC AND BEYOND

GOH KIAN HUI

NATIONAL UNIVERSITY OF SINGAPORE

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Declaration

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information chich have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Goh Kian Hui

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Abstract

Novel III-V Device Architectures

for Application in Future

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by

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The aggressive downscaling of complementary metal-oxide-semiconductor (CMOS) is facing great challenges due to fundamental limitations and practical considerations. To continue scaling beyond 14 nm technology node, various architectural and material changes in the traditional MOSFET would be required for efficient operation of the transistor as a switch. Among several emerging nanoscale devices, III-V MOSFETs are one of the most attractive devices due to their extremely high electron mobility. However, new processes associated with III-V substrates must be simplified, and costs of integration on Si substrate should be reduced. This thesis aims to address the various challenges in realizing short channel III-V MOSFETs on silicon for sub-7 nm logic applications.

First, ultra-thin-body (UTB) (1 nm-thick) $In_{0.53}Ga_{0.47}As$ channel junctionless n-FET with raised S/D structure and shortest reported gate length (L_G) of 6 nm was realized for III-V MOSFETs. Excellent control of short channel effects (SCEs) was achieved with I_{ON}/I_{OFF} ratio of

more than 10^5 and *DIBL* of 40 mV/V for devices with L_G down to sub-20 nm. Next, process for heteroepitaxial growth of high-quality $In_xGa_{1-x}As$ on Ge fin was developed. A physical modeling to describe the GaAs facets with different Ge fin orientation is proposed and verified experimentally.

To further improve device SCEs, a novel vertically stacked nanowire (NW) CMOS (InAs n-FET and GaSb p-FET) on Si platform was demonstrated using extremely thin buffer layer (sub-120 nm) technology. Our NW devices achieved the best reported I_{ON}/I_{OFF} ratio and swing for III-V CMOS integrated on silicon substrate. Finally, tapered S/D nanowire architecture and quantum dot with self-aligned S/D are demonstrated. These devices were fabricated by exploiting the III-V anisotropic wet etching and show promise to be adopted for future high performance and low power applications.

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List of Symbols

Symbol	Description	Unit
A_{NW}	Nanowire cross-sectional area	nm^2
B_{SAT}	Saturation ballistic ratio	
C_d	Depletion capacitance	F
C_{inv}	Inversion capacitance	$\mu F/cm^2$
C_{ox}	Gate oxide capacitance	F
C_G	Gate capacitance	$\mu F/cm^2$
C_S	Source junction capacitance	$\mu F/cm$
C_D	Drain junction capacitance	$\mu F/cm$
d	Etch depth	nm
D_{it}	Interface state density	$cm^{-2}eV^{-1}$
D_n	Diffusion coefficient for electron	cm^2s^{-1}
D_p	Diffusion coefficient for hole	cm^2s^{-1}
E_F	Fermi level	eV
E_C	Conduction band edge	eV
ΔE_C	Conduction band offset	eV
E_V	Valence band edge	eV
ΔE_V	Valence band offset	eV
ΔE_Γ	Subband energy separation in Γ-valley	eV
F	Filling factor	
g_{2D}	2D Density-of-states	$kg \cdot eV^{-2} \cdot s^{-2}$
G_M	Transconductance	$\mu S/\mu m$
$G_{M,peak}$	Peak transconductance	$\mu S/\mu m$
h	Planck's constant	eVs
H_{NW}	Nanowire height	nm
H_{SD}	Source/drain height	nm
I_D	Drive current (per unit width)	$\mu A/\mu m$
I_{Dlin}	Linear drain current (per unit width)	$\mu A/\mu m$
I_{OFF}	Off-state current	$\mu A/\mu m$
I_G	Gate current (per unit width)	$A/\mu m$
I_{ON}	On state current (per unit width)	$\mu A/\mu m$
I_{OFF}	Off state current (per unit width)	$A/\mu m$

k_B	Boltzman's constant	eV/K
L	Contact length	μm
L_C	Critical length	nm
L_D	Deybe Length	nm
L_{SD}	Spacing between source/drain and gate	nm
L_{EBL}	Electron beam lithography etch window opening size	nm
L_{EXT}	Nanowire extention region	nm
L_G	Gate length	Nm
L_T	Transfer length	μm
L_{CH}	Channel Length	nm
$L_{As\text{-}print}$	As-printed channel Length	nm
L_{SD}	Spacing between contact and channel	μm
m_{eff}	Effective mass	kg
m_t	Transverse mass	kg
m_l	Longitudinal mass	kg
m_{HH}	Heavy hole mass	kg
m_{LH}	Light hole mass	kg
m_0	Electron mass	kg
$\vec{n}_O$	Outward normal	
$\vec{n}_I$	Inward normal	
$\vec{n}_V$	Vertical normal	
N_A	Hole concentration	cm^{-3}
N_D	Electron concentration	cm^{-3}
N_S	Charge density	cm^{-3}
q	Electric charge	C
r	Growth rate	$nm \cdot s^{-1}$
R_{EXT}	Extrinsic series resistance	Ω·μm
R_C	Contact resistance	Ω·μm
R_{CH}	Channel resistance	Ω·μm
R_S	Source resistance	Ω·μm
R_D	Drain resistance	Ω·μm
R_{SD}	Source/drain series resistance	Ω·μm
R_T	Total resistance	Ω·μm

R_M	Metal Resistance	Ω·μm
SS	Subthreshold swing	mV/decade
t	time	s
T_M	Metal thickness	nm
T	Temperature	°C
T_{InGaAs}	InGaAs thickness	Nm
T_{NW}	Nanowire height	Nm
T_{ox}	Equivalent oxide thickness	nm
v_{ave}	Average velocity	$cm \cdot s^{-2}$
v_{Tx}	Unidirectional Thermal Velocity	$cm \cdot s^{-2}$
v_{x0}	Injection velocity	
V_G	Gate voltage	V
V_D	Drain voltage	V
V_{DD}	Common drain voltage	V
V_T	Threshold voltage	V
V_{TH}	Thermal Voltage	V
W_{EBL}	Spacing of electron beam lithography pattern	μm
W_{QD}	Spacing of parallel electron beam lithography pattern	nm
W_{NW}	Nanowire width	nm
x	Channel depth	nm
ε	permittivity	F/m
θ	Mask or fin orientation	°
ρ_C	Specific contact resistivity	$\Omega \cdot cm^2$
ρ_M	Specific metal resistivity	$\Omega \cdot cm^2$
ρ_{SD}	Specific semiconductor resistivity	$\Omega \cdot cm^2$
λ	Mean free path	nm
λ_{LIN}	Mean free path in the linear-regime	nm
λ_{SAT}	Mean free path in the saturation-regime	nm
μ_{app}	Apparent mobility	$cm^2\ V^{-1}s^{-1}$
μ_{bal}	Ballistic mobility	$cm^2\ V^{-1}s^{-1}$
μ_{eff}	Effective mobility	$cm^2\ V^{-1}s^{-1}$
μ_e	Electron mobility	$cm^2\ V^{-1}s^{-1}$
μ_h	Hole mobility	$cm^2V^{-1}s^{-1}$

$\lvert\Psi\rvert^2$	Electron probability	
ε_s	Permittivity	F/m
Φ_s	Surface potential	eV

Chapter 1

Introduction

1.1 Silicon Transistor Scaling: Benefits and Challenges

Phenomenal progress of transistor performance improvement and number of devices on chip quadrupling every three years signified by Moore's law has been achieved through geometrical scaling of metal-oxide-semiconductor field-effect transistor (MOSFETs) since 1960 [1]. Historically, the transistor current and operating voltage also scale in tandem with geometry to keep overall power density constant-codified as Dennard scaling [2]. However, Dennard scaling came to an abrupt end in 2005 due to increasing seriousness of short channel effects. The introduction of strained silicon [3]-[7], high-*k*/metal gate [8]-[10], and fin architecture in MOSFETs [11], [12] has been critical breakthroughs in advancing transistor technology in the last decade. However, continuous scaling of device dimensions and gate pitch pose new challenges to the conventional techniques and materials used for Si complementary metal-oxide-semiconductor (CMOS) strain engineering, especially when the technology node reaches 7 nm and beyond. Therefore, the advancement of future CMOS technology will rely increasingly on the innovative employment of materials, processes, and device architectures.

1.2 III-V Materials: Prospects and Challenges

In order to achieve high drive current at low supply voltage, the channel materials with high mobility and low effective mass are preferable [13]-[17]. For devices operating in quasi-

Table 1.1 Carrier mobility, effective mass, bandgap, and permittivity of various semiconductors [18].

	Si	Ge	$In_{0.53}Ga_{0.47}As$	InAs	InSb	InP	GaSb
Electron mobility (cm^2/Vs)	1350	3900	14000	33000	77000	5400	5000
Hole mobility (cm^2/Vs)	460	1900	400	460	850	200	850
Electron effective mass ($/m_0$)	m_t/m_l, 0.19/0.16	m_t/m_l, 0.082/1.467	0.05	0.027	0.013	0.08	0.042
Hole effective mass ($/m_0$)	m_{HH}/m_{LH}, 0.53/0.16	m_{HH}/m_{LH}, 0.35/0.043	m_{HH}/m_{LH}, 0.36/0.026	m_{HH}/m_{LH}, 0.37/0.043	m_{HH}/m_{LH}, 0.53/0.16	m_{HH}/m_{LH}, 0.55/0.083	m_{HH}/m_{LH}, 0.38/0.043
Bandgap (eV)	1.12	0.66	0.74	0.36	0.17	1.34	0.72

ballistic regime, the on-current (I_{ON}) is affected mainly by the injection velocity and backscattering coefficient. A lower effective mass along the channel transport direction would lead to higher injection velocity, irrespective of Fermi velocity [15], [19]. In addition, it had also been theoretical and experimentally demonstrated that low-field mobility is still a good indicator for high drive current under quasi ballistic transport regime [15].

As seen from Table 1.1, InGaAs, InP, and InSb are suitable channel materials for n-channel field-effect-transistors (nFETs) due to their high electron mobility and light electron effective mass. Meanwhile, GaSb, InGaSb, and InSb are potential candidates for p-channel field-effect transistors (pFETs) due to their high hole mobility and light hole effective mass. Therefore, there is a strong motivation to realize III-V CMOS on Si substrate for future high performance and low power logic applications.

However, there are still many critical issues and difficult challenges that need to be overcome before III-V transistors become viable for sub-7 nm technology node [18]. First, bulk III-V substrates are costly and difficult to make in large wafer sizes. Therefore, III-V materials have to be integrated on silicon substrates for low cost and high volume production. Second,

besides the requirement of a cost-effective and high-quality III-V material integration on silicon substrate, the integrated epi-layers should also be suitable for the fabrication of ultra-short channel devices and realization of both nFETs and pFETs with high device density. Thirdly, challenges such as formation of high-quality gate stack with low interface trap density, small equivalent oxide thickness (EOT), and low gate leakage need to be addressed. Last but not least, formation of source/drain (S/D) with low resistivity and low junction leakage are also very important. Fig. 1.1 summarizes the technical challenges which will be discussed and summarized in the following Sections.

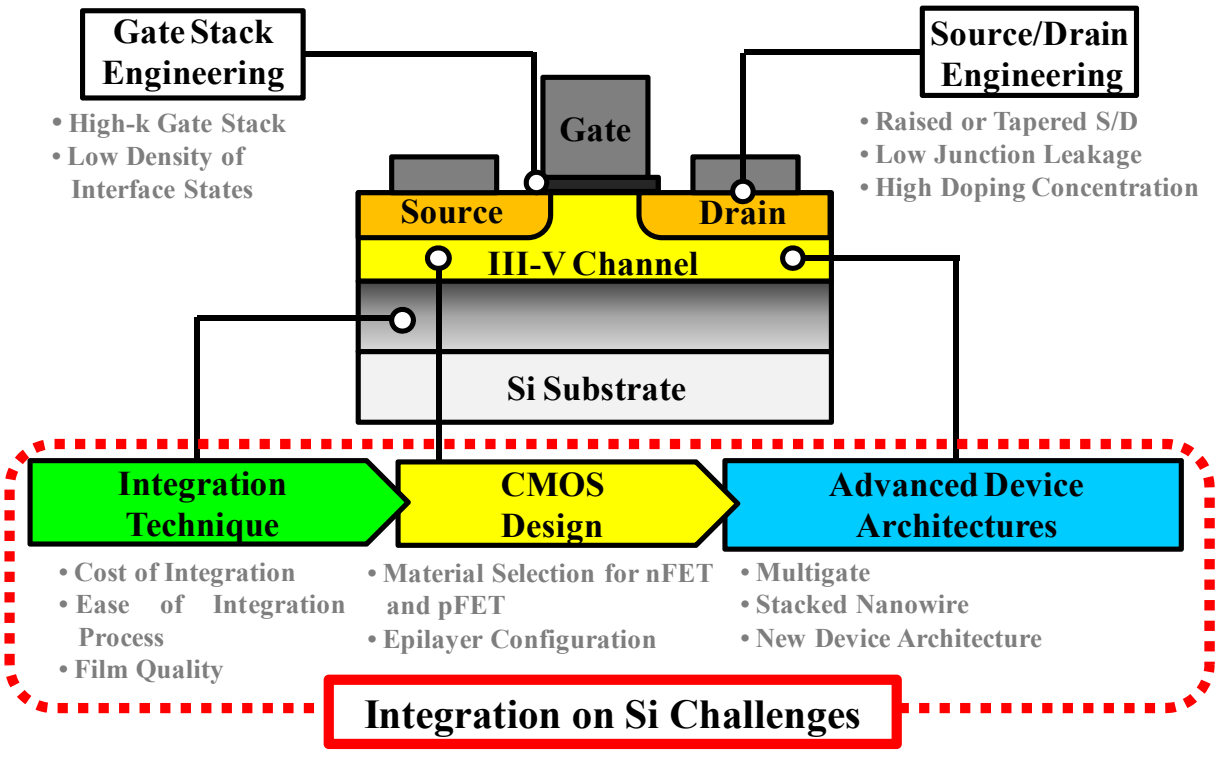


Fig. 1.1 Schematic illustration of the key technical challenges faced in the realization of high mobility III-V CMOS on silicon substrates for future high performance and low power logic application.

1.2.1 Integration on Si Challenges

(i) Cost-Effective Integration of High-Quality III-V Material on Silicon

To date, there are various approaches reported for integrating III-V materials on Si. Direct epitaxial growth of III-V materials on Si nanostructures [20] or often called as nanoheteroepitaxy technique is one of the simplest and cost-effective integration approaches. Nanoheteroepitaxy exploits the 3D stress relief mechanism when an epi-layer is nucleated on strain-compliant nanostructure in order to extend the critical thickness of the epi film drastically [34]. However, this approach has many disadvantages such as large mismatch in thermal expansion coefficient, non-intentional background doping of Si shallow impurities in III-V, and the formation of polar/non-polar interfaces between III-V and Si which compromises the quality of the as-grown III-V layers.

These challenges can be addressed by the use of graded buffer layer growth between Si and III-V layers to accommodate for the large lattice mismatch and reduce the number of defects reaching the active device layers [21], [22] Although high-quality III-V channel with moderate defect densities ~ 4×10^6 cm^{-2} were realized on Si, excessively thick graded buffer layer of more than 1 μm is typically required in the reported works, leading to high production cost. The buffer layer thickness needs to be aggressively reduced in order for this approach to be cost-effective.

Recently, aspect ratio trapping (ART) technique [23] has shown much promise as a cost-effective integration approach. ART employs selective III-V material growth in shallow trenches to confine the propagation of threading dislocation from reaching the active device layer. Significant progress using this approach, including demonstration of InGaAs FinFETs on Si substrates [24], has been made in recent years. However, ART technique cannot confine the

threading dislocations which are oriented along the trench direction from reaching the active layer, thus further improvement in the film quality of III-V channels is required.

Layer transfer is another promising technique to integrate III-V materials on Si substrate [25]. The advantages of layer transfer over other growth techniques are (1) high-quality III-V on insulator (III-V-OI) on Si can be achieved due to optimized growth condition, and (2) ease of realizing advanced device architectures such as multi-gate MOSFETs. However, the cost of this approach is a major concern [26].

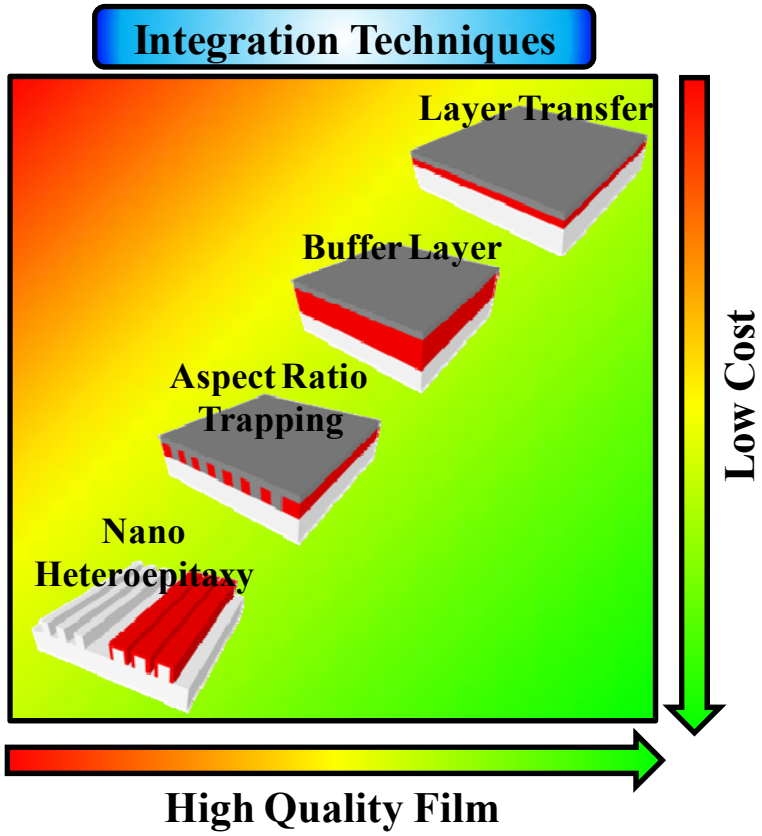


Fig. 1.2 Comparison of cost and film quality for the state-of-art integration techniques including layer transfer, buffer layer, nanoheteroepitaxy, and ART.

Fig. 1.2 compares the relative cost and film quality of various approaches of integrating III-V materials on Si, including layer transfer, ART, nanoheteroepitaxy, and buffer layer techniques. At the moment, the various integration techniques exhibit a trade-off between cost and film quality. This fuels for the search for new integration techniques which are cost effective and are able to achieve high-quality III-V channel layers.

(ii) High Density III-V CMOS on Si Substrate

From Table 1.1, it can be seen that III-V materials that are suitable for nFETs and pFETs are different due to their significant difference in electron and hole mobilities. Hence, two different III-V channel materials should be required for CMOS implementation. However, integrating high density nFETs and pFETs using two different channel materials could greatly complicate the fabrication process. Therefore, innovative CMOS design is required in order to achieve high density CMOS devices on Si.

Fig. 1.3 compares the strength and weaknesses of various III-V CMOS on Si designs that had been demonstrated or proposed to date. Among the various designs, single channel CMOS design such as InGaSb [27] offers the most straight-forward approach for CMOS implementation. InGaSb exhibits both high electron and hole mobilities, thus is suitable for both nFETs and pFETs. However, the state-of-art InGaSb nFETs still suffer from poor gate stack and high contact resistance due to Fermi level pinning near the valence band of InGaSb.

On the other hand, high performance CMOS can be realized by integrating As-based III-V nFETs with Sb-based III-V pFETs through double layer transfer technique [28]. This approach was first demonstrated by Nah *et al.* using the combination of InAs nFETs with InGaSb pFETs on Si substrates. However, the approach is not scalable and is very challenging to be applied to sub-7 nm technology node. A more viable approach would be to stack two

different channel materials on top of each other as demonstrated by IBM [29]. While this approach can realize high density CMOS devices with relatively simple integration approach, the step height between nFETs and pFETs is high and could increase the parasitic resistance and capacitance.

A modified version of stacked III-V layers, where two different channel materials are directly grown on top of each other could resolve the step height issue. Recently, M. Yokoyama *et al.* had demonstrated GaSb/InAs-OI bilayer CMOS heterostructures [29] using layer transfer technique. However, the devices exhibit serious ambipolar characteristics and devices with good performance have yet to be demonstrated.

ART technique is a promising approach that has the potential of co-integrating two different channel materials on Si for CMOS implementation. High performance InGaAs n-FinFETs [24] and Ge p-FinFETs [31] based on ART technique had been independently demonstrated. However, how to co-integrate two different channel materials in a cost effective way for sub-7 nm technology node is one of the main issues that ART needs to overcome.

Nanoheteroepitaxy is another promising approach that can be employed to directly integrate two different channel material on nano-patterned Si substrate [32], [33]. However, while it had been theoretically predicted that large lattice-mismatched III-V material such as InGaAs can be integrated on Si through nanoheteroepitaxy, growth of high-quality material has yet to be demonstrated. In addition, III-V materials that can be integrated on Si are very limited due to critical thickness constraint. For example, InSb and GaSb have superior mobility but cannot be integrated on Si directly through nanoheteroepitaxy.

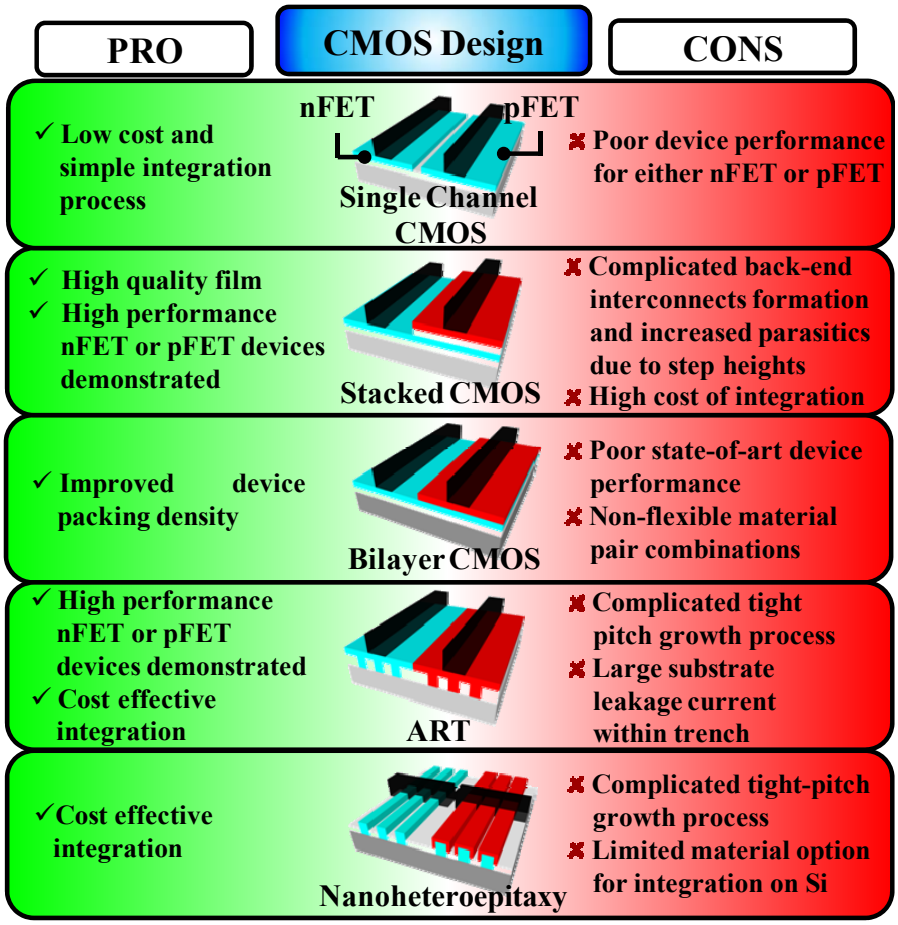


Fig. 1.3 Schematic illustrating the various CMOS on Si designs demonstrated and proposed to date.

(iii) Ultimate Device Architectures Realization for Sub-7 nm Technology Nodes

Another main challenge for implementing III-V CMOS in advanced technology nodes is the suppression of short-channel effects (SCEs). In present day, this was achieved by employing ultra-thin body (UTB) or FinFET structure. As compared with planar devices, FinFETs were introduced for silicon CMOS at the 22 nm technology node and had been shown to provide better control of SCEs, enhanced volume inversion in the channel region, lower leakage current, and reduced device variability arising from random dopant fluctuation [11], [12].

To sustain the continuous device miniaturization beyond 7 nm technology node, architectures such as multigate and stacked nanowire maybe required to improve the performance of extremely-scaled devices, as shown in Fig. 1.4. Such architectures have been shown to significantly improve the electrostatics control to achieve smaller SS and drain induced barrier lowering (DIBL). Consequently, better scalability can be realized as compared with fin structures [35].

Therefore, in order to effectively suppress SCEs in sub-7 nm technology node, the integration techniques and CMOS designs have to also account for the feasibility of realizing advanced device architectures. For instance, UTB structure can be easily realized by layer transfer technique. Meanwhile, ART technique allows for easy realization of fin structure. Moving forward, stacked nanowire structure is highly desirable. However, stacked nanowire structure cannot be easily realized by current integration techniques and CMOS designs.

Furthermore, as we approach 5 nm technology node and beyond, the ever increasing transistor number on single chip will require aggressive scaling of supply voltage to reduce energy consumption. This requires the exploration of novel device concept that can supplement the current CMOS devices. Possible candidates could be zero dimension (0D) single-electron transistors (SETs) [36], [37] and steep slope transistors which can operate at very low supply voltage such as source-filter FET and tunneling FET (TFET) [38].

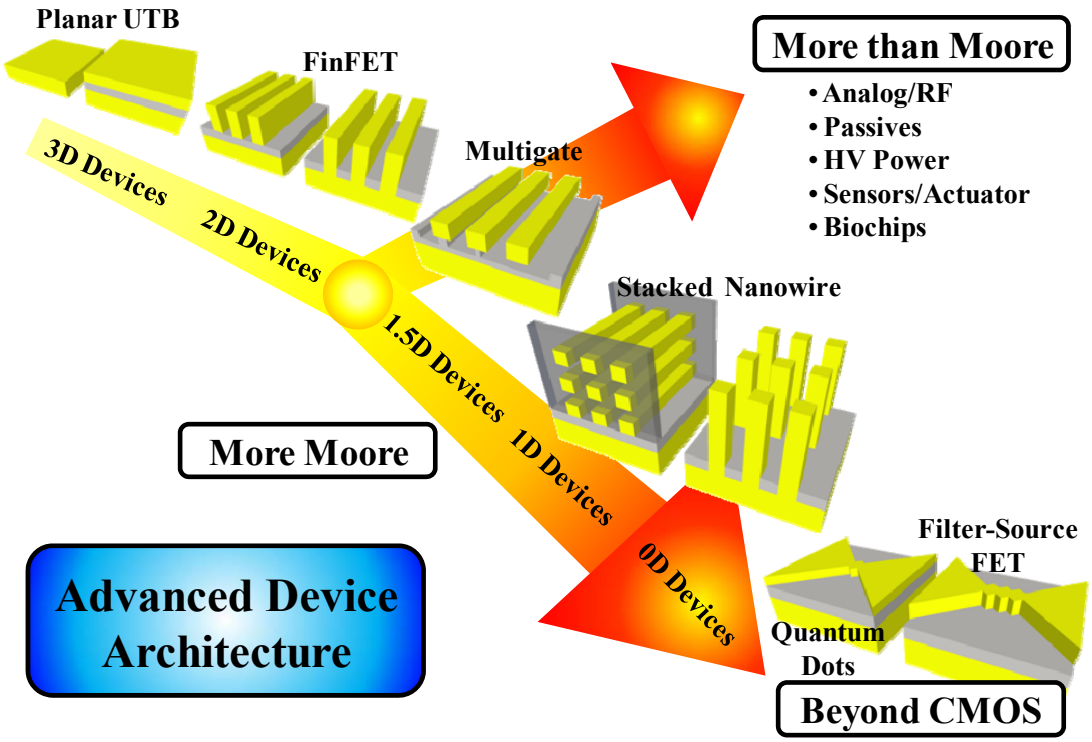


Fig. 1.4 Schematic illustrating the possible roadmap for advanced device architectures beyond 7 nm technology node. "More Moore" route emphasizes on the continuous miniaturization of device dimensions, potentially employing multigate and stacked nanowire architectures for effective SCEs control. Beyond 5 nm technology node, new device architecture such as single electron transistor (SETs), source-filter FETs and TFET could be explored. At the same time, "More Than Moore" route emphasizes on the diversification of device functionality on chip such as integration of analog, RF, passives, high voltage (HV) power devices, sensor and actuators on Si substrate.

1.2.2 High-k/Semiconductor Interface Quality

Intensive studies had revealed that III-V MOS interfaces normally have high density of interface states (D_{it}) [39], [40]. The origin of the high D_{it} can be attributed to the poor properties of III-V native oxides [41], [42]. Thus, III-V gate stack technologies for high-quality MOS interface are very important. Recently, an important discovery to achieve good quality high-*k*/III-V interface is depositing Al_2O_3 or HfO_2 using atomic layer deposition (ALD). The origin of

D_{it} reduction during ALD-deposited Al_2O_3 is attributed to the cleaning effect of trimethylalluminum (TMA) on the III-V surfaces [43], [44].

However, the reported Dit values on various MOS devices are still higher than 1×10^{11} $cm^{-2}eV^{-1}$ [18], and further reduction of D_{it} is still needed. In addition, as the III-V channel thickness becomes extremely scaled for sub-7 nm technology node, studies on the impact of interface traps on device performance under strong quantum confinement are important, but still lacking.

1.2.3 Source/Drain Engineering

The formation of S/D junction with low S/D series resistance and low leakage current is another critical issue in III-V MOSFETs. One of the challenges faced by III-V material is their difficulty to form highly doped S/D by conventional ion implantation method. This is because of the low solid solubility limitation of most III-V materials [45]. Furthermore, high temperature annealing cannot be employed due to the degradation of high-*k*/semiconductor interface at temperature above 600 °C. Therefore, epitaxial S/D with in-situ doping technique which can achieve the doping concentration higher than the thermal solubility limit is often adopted.

However for non-planar structure, the narrow fin or nanowire structure often leads to high resistance in the S/D extension regions. Self-aligned metal S/D techniques [46]-[50] which form a "salicide-like" metal contact next to the gate will be crucial for resistance reduction. Despite that, further S/D engineering are still required to boost the performance of nanowire for application beyond sub-7 nm technology node.

1.3 Objectives and Outline of the Thesis

The main objective of this dissertation is to address the challenge of integrating III-V MOSFETs on Si substrate. Cost-effective growth of high-quality III-V materials on Si substrate, novel CMOS design using III-V channel materials, and demonstration of advanced device architectures will be covered.

In Chapter 2, we realized junctionless FET (JLFET) featuring InP (1 nm)/ $In_{0.53}Ga_{0.47}As$ (1 nm)/InP composite channel with the shortest reported channel length L_{CH} of 6 nm for any III-V transistors. Excellent control of SCEs was achieved for JLFETs devices down to 20 nm L_{CH}. A detailed first-principle calculation and ballistic transport analysis were subsequently performed on these devices to extract various transport parameters.

In Chapter 3, we performed nanoheteroepitaxial growth of GaAs on Ge fins. A physical modeling of the growth is proposed and experimentally verified. Our physical model was able to explain the shapes of GaAs crystals grown on the Ge fins having different in-plane orientations. We subsequently optimized the growth process for nanoheteroepitaxy of $In_{0.2}Ga_{0.8}As$ on Ge fins. The successful growth and understanding of the (In)GaAs growth on Ge fin pave way towards integration of InGaAs n-channel FinFETs and Ge p-channel FinFETs on Si platform.

In Chapter 4, we demonstrated a novel vertically stacked III-V nanowire (NW) CMOS on Si substrate. The InAs nFETs and GaSb pFETs were integrated on a common Si platform using a cost-effective extremely-thin (sub-150 nm) buffer layer technology for the first time. Decent transfer characteristics were achieved with both InAs and GaSb devices having I_{ON}/I_{OFF} order of more than 3 orders. The effect of InAs nanowire thickness on the electrical characteristics of the InAs nanowire FETs was also investigated by simulation and experiment.

In Chapter 5, we exploit the III-V wet etch profile to realize novel device architectures beyond the conventional CMOS. A physical modeling of the wet etch was first proposed and verified through extensive experimental results. Subsequently, the anisotropic wet etch profile was employed to realize novel device architectures such as junctionless nanowire with tapered S/D structure and quantum dot with self-aligned S/D structure for the first time.

Finally, the main contributions of this thesis and suggestions for future work are summarized in Chapter 6.

Chapter 2

Sub-7 nm Channel Length Junctionless FETs (JLFETs) with Band-Engineered InP/In0.53Ga0.47As/InP for Improved Density-Of-States (DOS)

2.1 Introduction

High-mobility InGaAs could replace Si as the channel material for high performance and low power logic applications in sub-10 nm technology node [51]-[60] due to its high injection velocity. However, InGaAs suffers from low density-of-states (DOS), and consequently provides diminishing benefit over Si as the effective oxide thickness (EOT) is scaled below 0.6 nm where the effect of quantum capacitance becomes more important [61]-[63].

Various approaches to increase the DOS of InGaAs have been explored. One approach is to explore the quantum confinement effect of the extremely scaled channel thickness to increase the DOS effective mass. However, the strong quantum confinement effect also leads to significant degradation of the carrier velocity [64]-[66].

Strain engineering [67]-[71] which have been widely employed in Si can also be utilized to modify the semiconductor band structure. However, strain effect is less effective for InGaAs n-channel field-effect transistors (nFETs) due to the large inter-valley separation between Γ-valley and L-valley and the isotropic nature of the InGaAs conduction band at the Γ-valley [72].

Recently, alternative III-V channel materials, such as GaSb, have also been investigated to take the advantage of higher DOS due to their small energy separation between Γ-valley and L-valley [73]. Nevertheless, the realization of high performance GaSb nFETs is still very challenging due to the poor interface quality between gate dielectrics and GaSb as well as the high contact resistance in the S/D regions. This is because of the Fermi level (E_F) pinning towards the valence band edge of GaSb [74]-[77].

In this Chapter, we perform a detailed analysis on InP/$In_{0.53}Ga_{0.47}As$/InP heterostructure as shown in Fig. 2.1 (a) using $sp^3d^5s^*$ tight-binding (TB) model. We found that $In_{0.53}Ga_{0.47}As$ thickness (T_{InGaAs}) plays an important role in engineering of the band-edge DOS of InP/$In_{0.53}Ga_{0.47}As$/InP. We define such heterostructure as band-engineered channel heterostructure (BCH) in this Chapter. As compared with the conventional InGaAs single channel material, the subband energy separation in the Γ-valley (ΔE_Γ) of the InP/$In_{0.53}Ga_{0.47}As$/InP BCH reduces with decreasing T_{InGaAs}, leading to enhancement in the band-edge DOS. At the same time, very small degradation in carrier velocity was observed for InP/$In_{0.53}Ga_{0.47}As$/InP BCH.

We examine the electrical performance of InP/$In_{0.53}Ga_{0.47}As$/InP BCH using the semi-classical top-of-barrier (TOB) model in Section 2.2. In Section 2.3, the short-channel InP/$In_{0.53}Ga_{0.47}As$/InP BCH devices with L_{CH} down to 6 nm [78] were realized and characterized. Subsequently, detailed analysis was performed in Section 2.3 to extract the unidirectional thermal velocity (v_{Tx}), critical length (L_C), and mean free path (λ) in linear and saturation regime using the method proposed by MIT [79].

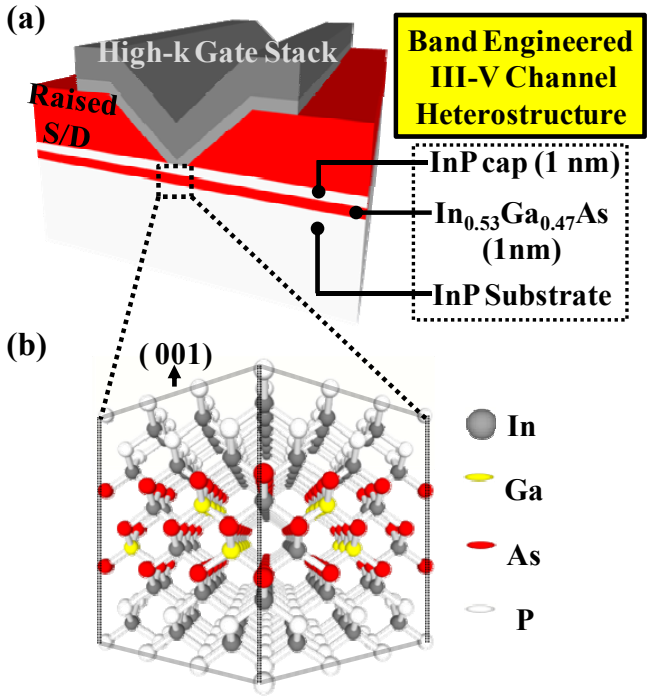


Fig. 2.1 (a) Schematic of a III-V JLFET featuring InP(1 nm)/$In_{0.53}Ga_{0.47}As$(1 nm)/InP BCH, highly doped n++ raised S/D structure (5×10^{19} cm^{-3}), and high-k gate stack. (b) Atomic representation of the InP/$In_{0.53}Ga_{0.47}As$/InP BCH, which is a zinc blende structure with (001) surface orientation.

2.2 Simulation of Band-Engineered InP/$In_{0.53}Ga_{0.47}As$/InP Devices

2.2.1 Band Structure Calculation of InP/$In_{0.53}Ga_{0.47}As$/InP BCH

The band structures of the InP/$In_{0.53}Ga_{0.47}As$/InP BCH with 1-5 nm T_{InGaAs} were simulated using the $sp^3d^5s^*$ tight-binding (TB) model with consideration of the effect of spin-orbit coupling. The $sp^3d^5s^*$ model only need nearest neighbor interaction which can reduce the computational cost, unlike the sp^3 model which require multiple nearest neighbor interaction to get the band structure correctly. Furthermore, the s* is used for including electron coupling for excited states in order to provide the more accurate effective mass at E_c [80]. The inclusion of the excited s-state s^* on each atom repels the lower, unoccupied energy levels of the neighboring atom and presses the relative conduction band minima down in energy. The tight-binding

parameters for InP and InGaAs have been optimized, and are taken from reference [81]-[82]. Fig. 2.1 (b) shows the zinc blende atomic representation of the InP/$In_{0.53}Ga_{0.47}As$/InP BCH. In order to account for the channel surface band bending effect due to the gate bias, our simulation adopted an approximation of the band profile given by the equation

$$\Phi_S(x) = \Phi_S \exp(-\frac{x}{L_D}), \tag{2.1}$$

where L_D is the Deybe length and is given by

$$L_D = \sqrt{\frac{\varepsilon k_B T}{q^2 N_A}}. \tag{2.2}$$

In equation (2.1) and (2.2), x is channel depth, Φ_S is the surface potential, ε is the permittivity of the channel material, k_B is Boltzmann constant, T is temperature, q is electron charge, and N_A is the substrate doping concentration. The calculated Φ_S profiles as a function of x for various N_A is shown in Fig. 2.2 (a). In Fig 2.2 (b), the band diagram of the simulation structure is shown. In our TB calculation, the thicknesses of the InP cap and the InP substrate are fixed at 1 nm and 30 nm, respectively, while T_{InGaAs} varies from 1 to 5 nm. The substrate thickness of 30 nm was found to be sufficiently thick for the wavefunction of carrier from the surface to decay to a negligible value. For the parameters of channel surface band bending, Φ_S values from 0.1 to 0.5 eV and N_A of 1×10^{16}, 5×10^{16}, 1×10^{17}, and 1×10^{18} cm^{-3} were considered in our simulation.

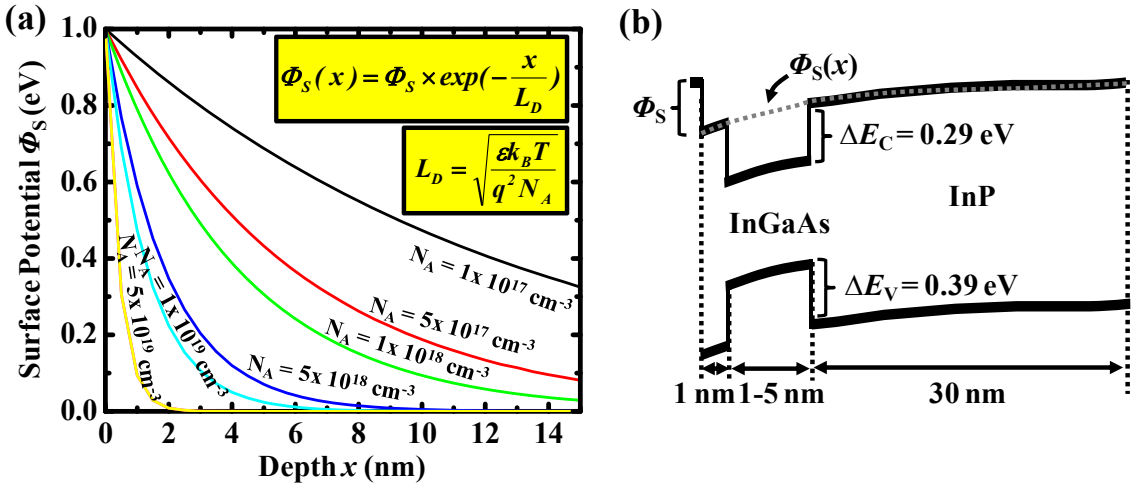


Fig. 2.2 (a) Plot of theoretical Φ_S versus depth (x). The inset shows the equation for Φ_S, where L_D is Deybe length, ε is permittivity, k_B is Boltzmann constant, T is temperature, q is electrical charge, and N_A is substrate doping concentration. (b) Energy band diagram showing the layer structure defined for our TB calculation.

Fig. 2.3 shows the energy dispersion (E-k) plots of InP/$In_{0.53}Ga_{0.47}As$/InP BCH with T_{InGaAs} from 1 nm (leftmost plot) to 5 nm (rightmost plot) for fixed N_A of 1×10^{18} cm^{-3}and Φ_S of 0.1 eV. For all the plots, the energy reference level is set at the valence band maxima of InP ($E_{V,INP}$ = 0 eV). As T_{InGaAs} decreases from 4 to 1 nm, the subband energy level within InGaAs quantum well (QW) increases due to stronger quantum confinement by the InP energy barrier. On the other hand, the second lowest subband energy level remains relatively unaffected by T_{InGaAs} since they are outside of InGaAs QW. This leads to a smaller subband energy separation (ΔE_Γ) in the Γ-valley of the InP/$In_{0.53}Ga_{0.47}As$/InP BCH structure with decreasing T_{InGaAs}. However, InP/$In_{0.53}Ga_{0.47}As$/InP BCH with 5 nm T_{InGaAs} does not follow a similar trend because the first two lowest subbands are within the InGaAs QW as shown in the rightmost plot of Fig. 2.3.

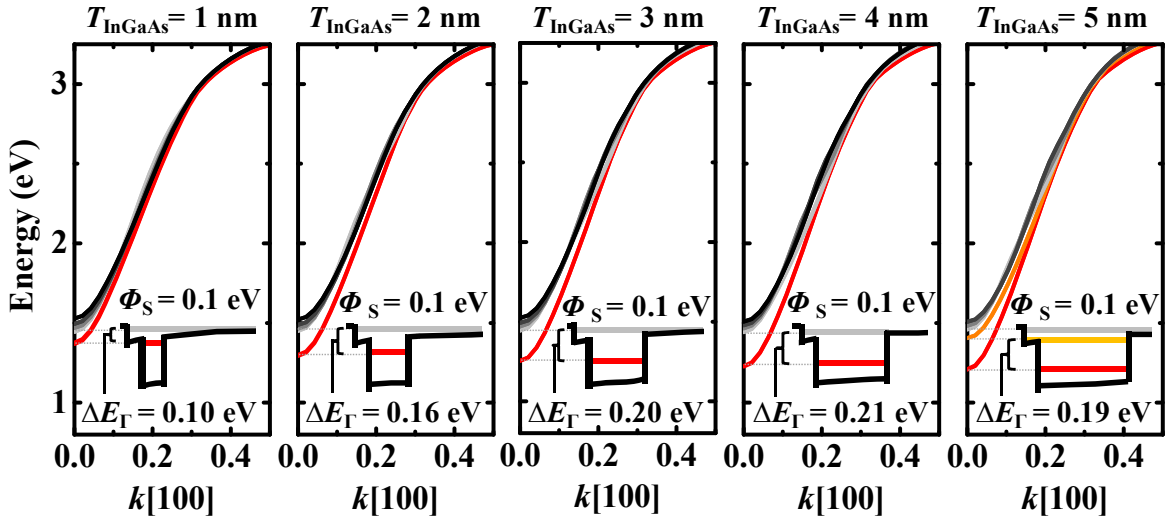


Fig. 2.3 Energy dispersion (*E-k*) showing the first 5 subbands in the conduction band of InP/$In_{0.53}Ga_{0.47}As$/InP BCH at Φ_S of 0.1 eV and N_A of 1×10^{18} cm^{-3}. T_{InGaAs} varies from 1 nm (leftmost plot) to 5 nm (rightmost plot). Insets show the subband energy level within the simulated channel QW. As T_{InGaAs} decreases from 4-1 nm, the subband energy level within InGaAs QW increases due to stronger quantum confinement by the InP energy barrier. The trend does not apply for InP/$In_{0.53}Ga_{0.47}As$/InP BCH with 5 nm T_{InGaAs} due to the existence of second subband within the InGaAs QW.

The plot of ΔE_Γ as a function of T_{InGaAs} is shown in Fig. 2.4 (a). It is important to note that, because of the small conduction band offset between $In_{0.53}Ga_{0.47}As$ and InP, confinement of the carriers in the $In_{0.53}Ga_{0.47}As$ layer is weak. Therefore, a small change of the effective mass (m_{eff}) was observed when T_{InGaAs} decreases from 5 to 1 nm as shown in Fig. 2.4 (b). In Fig. 2.4 (c), 2D DOS versus the energy level above their respective conduction band edge (E-E_C) for InP/$In_{0.53}Ga_{0.47}As$/InP BCH with T_{INGAAS} of 1-5 nm is shown. The 2D DOS is calculated by

$$g_{2D}(E) = \frac{m_{eff}}{\pi\hbar^2}, \tag{2.3}$$

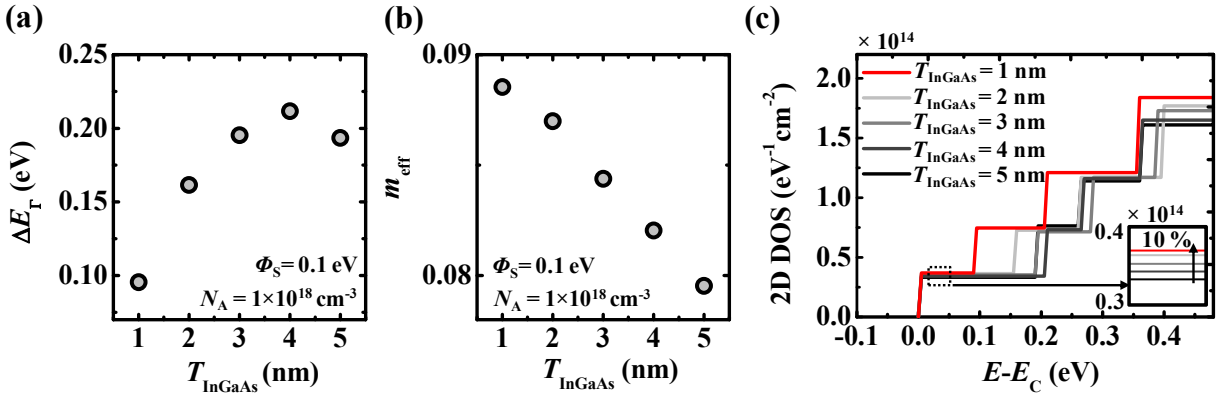


Fig. 2.4 Plot of (a) effective mass (m_{eff}) versus T_{InGaAs}, (b) ΔE_Γ versus T_{InGaAs}, and (c) 2D DOS versus the energy level above their respective conduction band edge (E-E_C) for InP/$In_{0.53}Ga_{0.47}As$/InP BCH with T_{InGaAs} of 1-5 nm. The plots correspond to the E-k diagram in Fig. 2.3 where Φ_S and N_A are fixed at 0.1 eV and 1×10^{18} cm^{-3}, respectively. The inset in (c) shows the zoom-in view of 2D DOS in the 0-0.05 eV range. Only a small increase of 2D DOS effective mass (10 %) was observed due to the weak carrier confinement.

where $\hbar$ is the reduced Plank constant and m_{eff} is the effective mass obtained by fitting the E-k plot in the Γ-valley assuming parabolic band. We found that the improvement of DOS due to the increase in effective mass is trivial (~10 %), as shown in the inset of Fig. 2.4 (c). The increase in DOS is mainly due to the contribution from the additional subband at the InP band-edge as the result of the decrease in ΔE_Γ between two lowest subbands.

The effect of Φ_S on the InP/$In_{0.53}Ga_{0.47}As$/InP BCH bandstructure is shown in Fig. 2.5. In the plot, the Φ_S varies from 0.1 eV (leftmost plot) to 0.5 eV nm (rightmost plot), while N_A and T_{InGaAs} are fixed at 1×10^{18} cm^{-3}and 3 nm, respectively. As Φ_S increases from 0.1-0.5 eV, the InP triangular QW becomes more prominent due to increasing barrier height. Therefore, the ΔE_Γ increases due to the stronger confinement of carriers by InP triangular QW. The plot of ΔE_Γ as a function of Φ_S for InP/$In_{0.53}Ga_{0.47}As$/InP BCH with T_{InGaAs} of 1-5 nm is shown in Fig. 2.6 (a). Obvious increase of ΔE_Γ with increasing Φ_S can be seen for InP/$In_{0.53}Ga_{0.47}As$/InP BCH with

T_{InGaAs} of 1 to 4 nm. In the case of InP/$In_{0.53}Ga_{0.47}As$/InP BCH with T_{InGaAs} of 5 nm, ΔE_Γ is

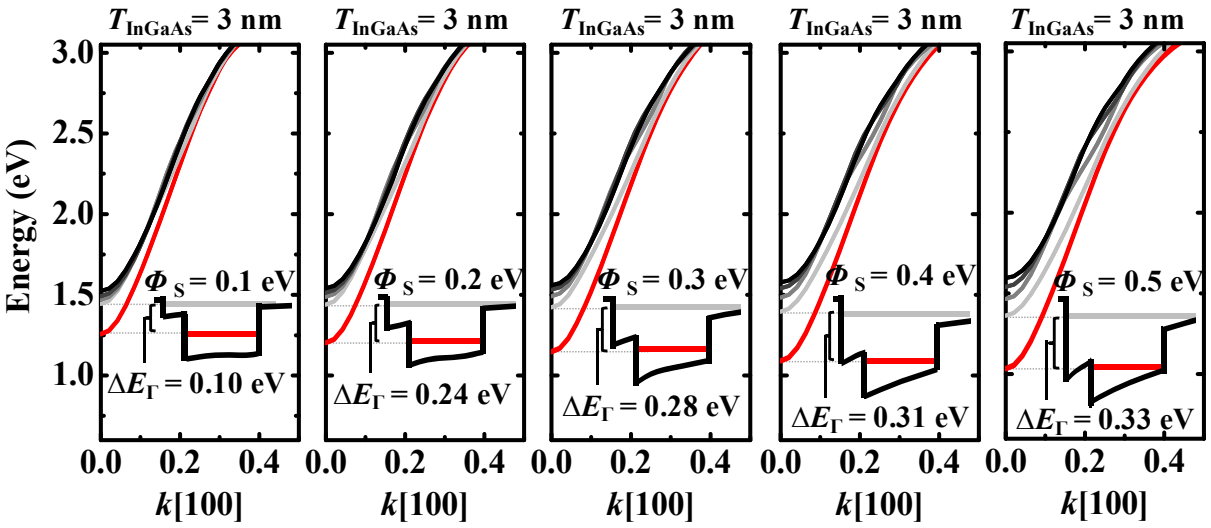


Fig. 2.5 Energy dispersion (*E-k*) showing the first 5 subbands in the conduction band of InP/$In_{0.53}Ga_{0.47}As$/InP BCH with T_{InGaAs} of 3 nm and N_A of 1×10^{18} cm^{-3}. Φ_S vary from 0.1 eV (leftmost plot) to 0.5 eV (rightmost plot). Insets show the subband energy level for the InP/$In_{0.53}Ga_{0.47}As$/InP BCH with consideration of surface band bending. The ΔE_Γ increases with increasing Φ_S due to the stronger quantum confinement effect of the triangular QW.

weakly affected by the change in Φ_S. This is because both the lowest two subbands reside within InGaAs QW. As compared to InP triangular QW, increasing Φ_S does not significantly alter the InGaAs QW width, thus the subband(s) within InGaAs QW is less sensitive to the effect of Φ_S.

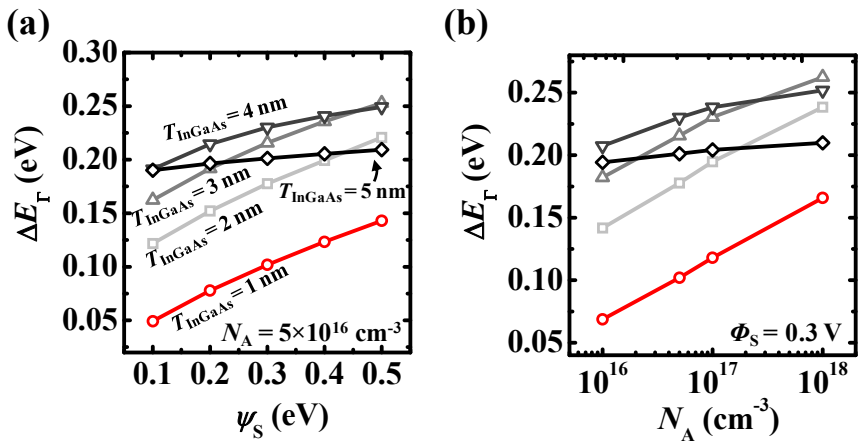


Fig. 2.6 Plot of (a) ΔE_Γ versus Φ_S and (b) ΔE_Γ versus N_A. In (a), the results are obtained at N_A of 5×10^{16} cm^{-3}, while in (b), the results are obtained at Φ_S of 0.3 eV.

In Fig. 2.6 (b), the plot of ΔE_Γ versus N_A at Φ_S of 0.3 eV shows a similar trend. This is because N_A impacts the InP/$In_{0.53}Ga_{0.47}As$/InP BCH bandstructure in a similar way as Φ_S, where higher N_A would lead to stronger confinement of carriers by InP triangular QW due to decreasing QW width.

2.2.2 Top-of-barrier Simulation of Transistors with InP/$In_{0.53}Ga_{0.47}As$/InP BCH

In this Section, semi-classical top-of-barrier (TOB) transport calculations were carried out to obtain the ballistic drive current (I_D) of the InP/$In_{0.53}Ga_{0.47}As$/InP BCH devices. The TOB calculations are based on the effective masses and energy levels of the subbands [80],[84]. 20 lowest subbands were considered in our TOB calculations. EOT and the drain voltage (V_D) are maintained at 0.5 nm and 0.5 V, respectively.

Plot of charge concentration (N_S) versus N_A at Φ_S of 0.3 eV is shown in Fig. 2.7 (a). It can be seen that N_S of 1 nm T_{InGaAs} device is superior to other devices in all the simulated N_A range. At N_A of 1×10^{16} cm^{-3}, significant enhancement in the charge density (N_S) of ~80 % can be seen for 1 nm T_{InGaAs} device as compared to 5 nm T_{InGaAs} device. This is due to the higher

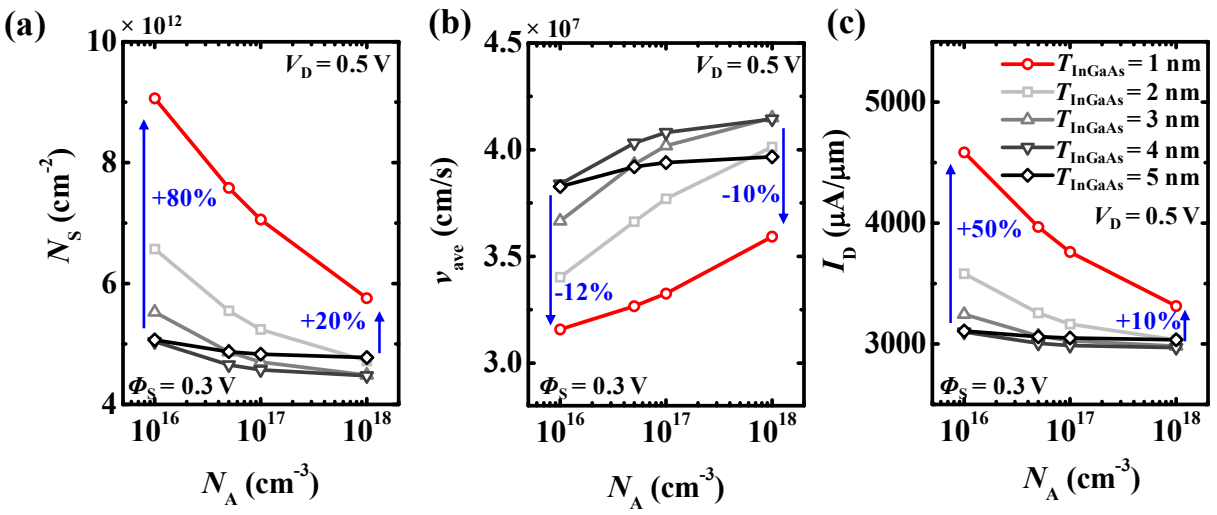


Fig. 2.7 TOB simulation of (a) charge density (N_S) versus N_A, (b) average velocity (v_{ave}) versus N_A, and (c) I_D versus N_A. In plot (a)-(c), Φ_S is maintained at 0.3 eV, while both T_{InGaAs} and N_A vary from 1 to 5 nm and 1×10^{16} to 1×10^{18} cm^{-3}, respectively. All the TOB simulations are performed at EOT of 0.5 nm and V_D of 0.5 V.

DOS of 1 nm T_{InGaAs} device owing to its small ΔE_Γ. Furthermore, only slight degradation (~12 %) in average velocity (v_{ave}) of carriers is observed [Fig. 2.7 (b)] due to the weak confinement of electron in $In_{0.53}Ga_{0.47}As$ QW by the InP barrier. However at higher N_A of 1×10^{18} cm^{-3}, the N_S enhancement of 1 nm T_{InGaAs} device over 5 nm T_{InGaAs} device reduces to 20%. This is consistent with the observation that ΔE_T increases with increasing N_A as discussed in previous sub-section. In Fig. 2.7 (c), the plot of I_D versus N_A is shown. The I_D is proportional to the product of N_S and v_{ave} as given by

$$I_D = qN_s v_{ave}, \tag{2.4}$$

where q is the electronic charge. Since scaling down of T_{InGaAs} leads to large gain in N_s and small drop in v_{ave}, I_D of InP/$In_{0.53}Ga_{0.47}As$/InP BCH devices with 1 nm T_{InGaAs} outperforms that of the 5 nm T_{InGaAs} by 50 % at N_A of 1×10^{16} cm^{-3} and 10 % at N_A of 1×10^{18} cm^{-3} as shown in Fig. 2.7 (c).

In conclusion, our simulation results show that InP/$In_{0.53}Ga_{0.47}As$/InP BCH is a promising structure to improve $In_{0.53}Ga_{0.47}As$ DOS since the ΔE_Γ can be engineered by T_{InGaAs}. Furthermore, the v_{ave} degradation with decreasing T_{InGaAs} is small. Based on the simulation results from this Section, JLFET devices with 1 nm T_{InGaAs} InP/$In_{0.53}Ga_{0.47}As$/InP BCH and undoped InP substrate (background doping, $N_A \sim 1\times10^{16} - 5 \times 10^{16}$ cm^{-3}) were fabricated in the next Section for further electrical characterizations and in-depth transport analysis.

2.3 Realization of InP/$In_{0.53}Ga_{0.47}As$/InP JLFETs

Fig. 2.8 (a)-(b) shows the process flow for the fabrication of InP/$In_{0.53}Ga_{0.47}As$/InP JLFETs. The starting substrate features 1 nm-thick $In_{0.53}Ga_{0.47}As$ layer sandwiched between 1 nm-thick InP capping layer and the InP (001) substrate with a 200 nm-thick heavily-doped n++ $In_{0.53}Ga_{0.47}As$ (5×10^{19} cm^{-3}) top layer. The InP capping layer and InP substrate are undoped while the 1 nm-thick $In_{0.53}Ga_{0.47}As$ is n-type doped with doping concentration of 1×10^{18} cm^{-3}. This substrate is purchased from IntelliEPI and the epi-layers are grown by molecular beam epitaxy (MBE). First, the mesa mask is defined by lithography, followed by wet etching in H_3PO_4:H_2O_2:H_2O (1:1:20 by volume) for 2 minutes at room temperature. After the mesa formation, rectangular-shaped etch windows with opening size (L_{EBL}) ranging from 50 to 280 nm were defined by electron beam lithography (EBL) along $[1\bar{1}0]$ direction on the patterned mesa. Anisotropic wet etch of n++ $In_{0.53}Ga_{0.47}As$ using H_3PO_4:H_2O_2:H_2O (1:5:20 by volume) for 15 s was then performed at room temperature. The H_3PO_4:H_2O_2:H_2O solution was calibrated to etch n++ $In_{0.53}Ga_{0.47}As$ at 13 nm/s with $In_{0.53}Ga_{0.47}As$ over InP selectivity of 1600:1. Due to the high etch selectivity, the etch stops at InP capping layer. This anisotropic wet etch of $In_{0.53}Ga_{0.47}As$ along the $[1\bar{1}0]$ direction exposes (111)A Ga-terminated surface, resulting in the formation of V-

Groove, as shown in the tilted-view scanning electron microscopy (SEM) image in Fig. 2.8 (c). This is an essential step to achieve a transistor with sub-10 nm LCH.

After that, the gate stack was formed which comprises of 5 nm Al2O3 gate dielectric deposited by atomic layer deposition (ALD) and 100 nm TaN deposited by sputter. Top SEM view of the completed JLFET device is shown in the Fig. 2.8 (d). The sample was next patterned by lithography for metal contact formation on the S/D region. A quick dip into diluted hydrofluoric acid (1:100) was performed for native oxide removal. This was immediately followed by Pd (40 nm) and Ge (90 nm) deposition process to form Pd/Ge metal pads. Annealing at 400 °C for 10 s was then performed for PdGe Ohmic contact formation. The annealing process would allow Ge to diffuse down to react with Pd and excess Ge would

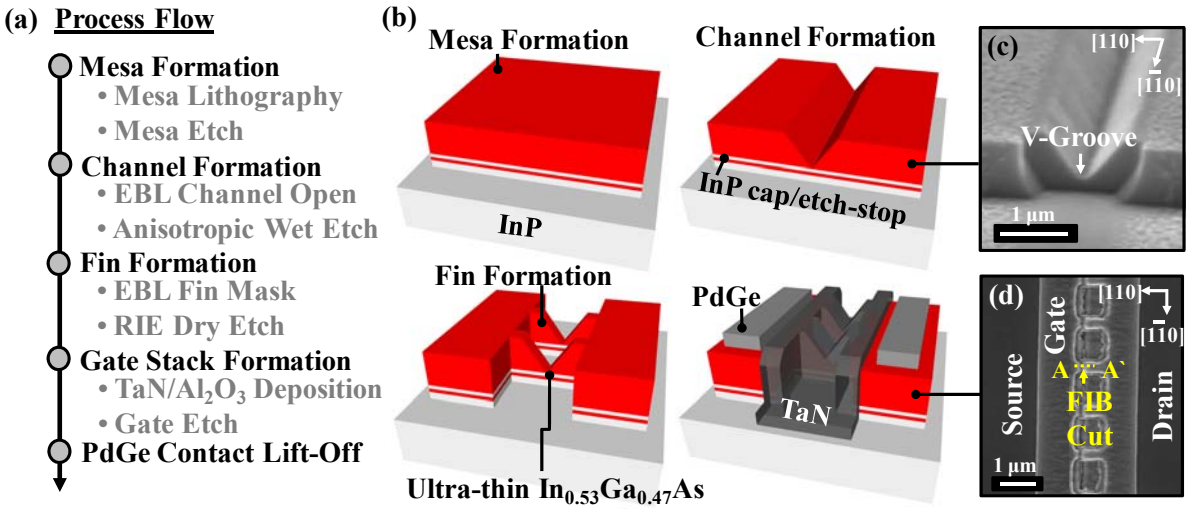


Fig. 2.8 (a) Key process flow for fabrication of ultra-short channel (~ 6 nm) JLFET. (b) 3D schematics illustrate the mesa formation step, channel formation step (with ultra-thin InP cap as etch-stop), fin formation step, and the completed device structure after gate stack and PdGe contact lift-off step. (c) Tilted-view SEM image of the V-Groove formed during channel formation step which is critical to the formation of ultra-short channel JLFET devices. (d) Top SEM view of the completed device. FIB cut is performed along the A-A` for subsequent TEM characterization.

dope $In_{0.53}Ga_{0.47}As$ at PdGe/$In_{0.53}Ga_{0.47}As$ interface [85], [86]. The layout for the JLFET device fabrication can be found in appendix 2.7.1.

In Fig. 2.8 (d), focused ion beam (FIB) cut was performed along the A-A` direction in order to obtain the cross-sectional transmission electron microscopy (TEM) image in Fig. 2.9 (a). zoom-in view TEM image (bright-field) at the channel region in Fig. 2.9 (b) shows that the physical channel length of ~ 6 nm was achieved. All the TEM cross-sectional images are taken with zone axis (ZA) oriented to InP<110>. Scanning transmission electron microscopy energy-dispersive X-ray spectroscopy (STEM-EDX) elemental mapping of As K_α, Ga K_α, P K_α and In K_α in Fig. 2.9 (c) confirm the presence of the 1 nm-thick $In_{0.53}Ga_{0.47}As$ sandwiched between the 1 nm-thick InP capping layer and the InP substrate. High-angle annular dark field (HAADF) STEM is employed here using the FEI Tecnai X-TWIN TEM.

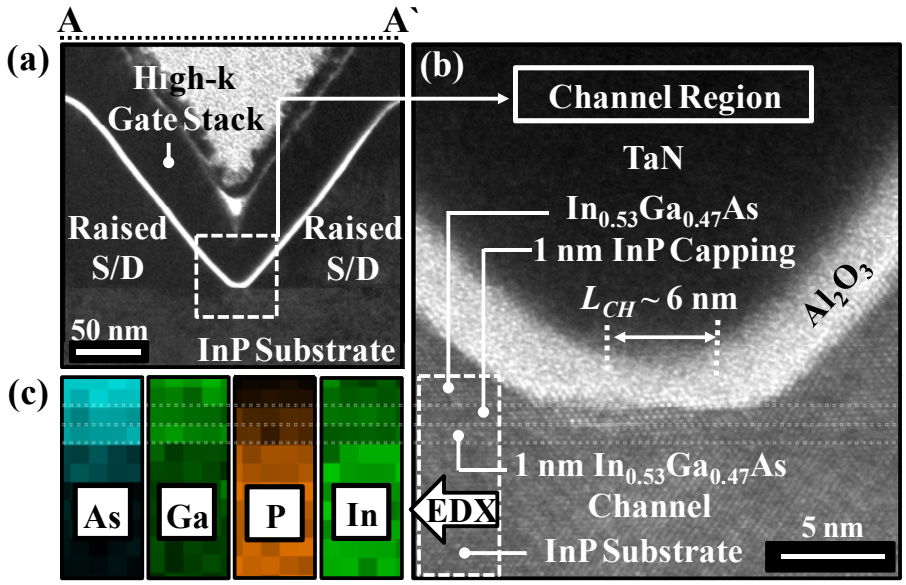


Fig. 2.9 (a) Cross-sectional TEM image along A-A` of a JLFET device in Fig 2.8 (c) showing V-Groove channel formed by anisotropic wet etch. (b) Zoom-in view of the channel region showing L_{CH} of ~ 6nm. The zone-axis (ZA) for all TEM images is [110] (c) STEM-EDX elemental mappings of the As K_α, Ga K_α, P K_α and In K_α on the channel region shows the presence of ultra-thin 1 nm InP capping layer and 1 nm $In_{0.53}Ga_{0.47}As$ thickness. The TEM and EDX are performed at Data Storage Institute (DSI) through a service contract.

2.4 Electrical Characterizations of InP/$In_{0.53}Ga_{0.47}As$/InP JLFET Devices

Fig. 2.10 (a) shows the I_D-V_G curves of InP/$In_{0.53}Ga_{0.47}As$/InP JLFET with L_{CH} of 6 nm. Decent transfer characteristics were observed. Drive current of 420 μA/μm was achieved at a gate over drive of 0.7 V and V_D of 0.7 V as shown in the output characteristics of the same device in Fig. 2.10 (b). I_D-V_G of a transistor with L_{CH} of 76 nm is shown in Fig. 2.10 (c). This device exhibited excellent short channel effect control with high I_{ON}/I_{OFF} of 5 orders and very good subthreshold characteristics with *DIBL* of 165 mV/V and subthreshold swing (*SS*) of 131 mV/decade at V_D of 0.7 V.

The excellent control of SCEs was also depicted in the plots of *DIBL* versus L_{CH} and threshold voltage (V_T) versus L_{CH} at V_D of 0.5 V in Fig. 2.11. The V_T is extracted using linear extrapolation method at V_D of 0.05 V. The improved electrostatics down to sub-20 nm was achieved by using an extremely-thin $In_{0.53}Ga_{0.47}As$ channel. A similar enhancement was observed in the I_{ON}/I_{OFF} versus L_{CH} plot [Fig. 2.12] where I_{ON}/I_{OFF} of ~5×10^5 at V_D of 0.5 V was achieved for JLFETs down to sub-20nm L_{CH}. The plot of I_{ON} versus I_{OFF} in Fig. 2.13 shows that, at a fixed I_{OFF} of 1 μA/μm, the transistors delivered a drive current of 550 μA/μm at $V_G = V_D =$ 0.7 V. With further EOT scaling, the drive current and control of SCEs can be improved.

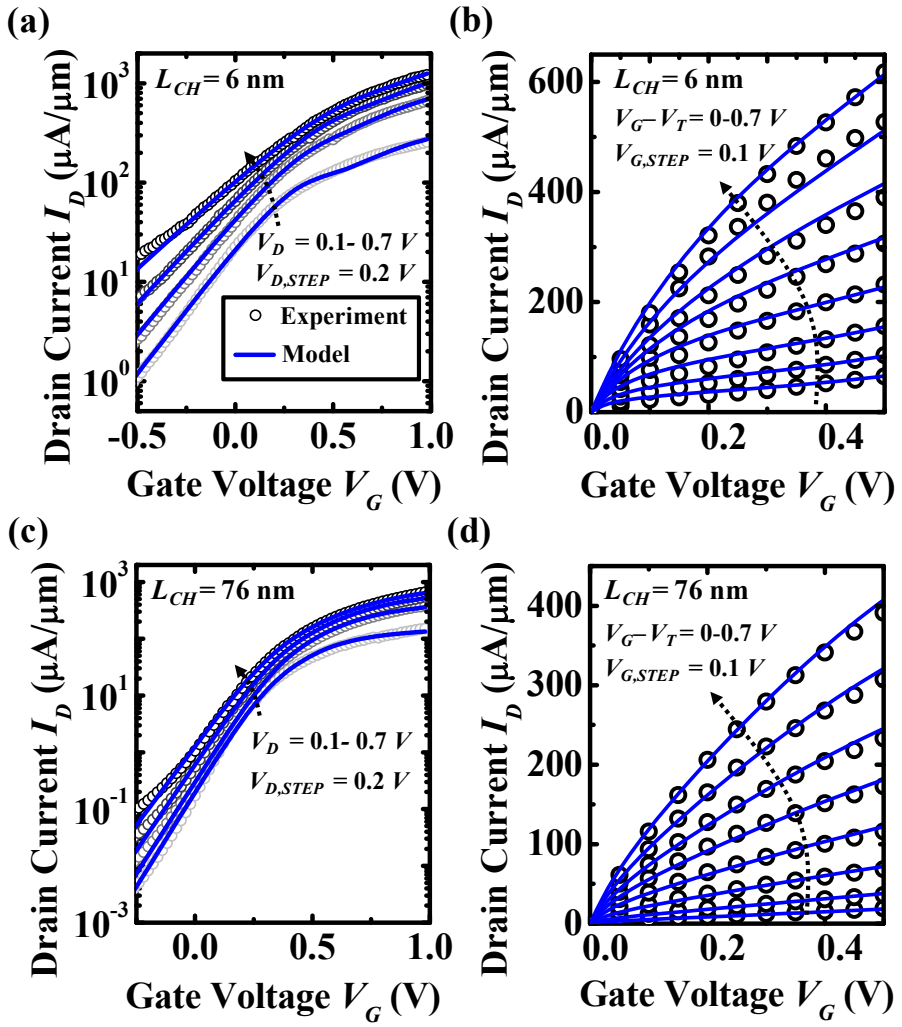


Fig. 2.10 Comparison of the measured InP/$In_{0.53}Ga_{0.47}As$/InP nFET data (symbols) and modeled data (lines) at room temperature for L_{CH} of 6 nm (top row) and L_{CH} of 76 nm (bottom row). Excellent data fitting by VS model was obtained for a wide range of L_{CH} and bias voltages using V_G independent values of v_{x0} and μ_{app}.

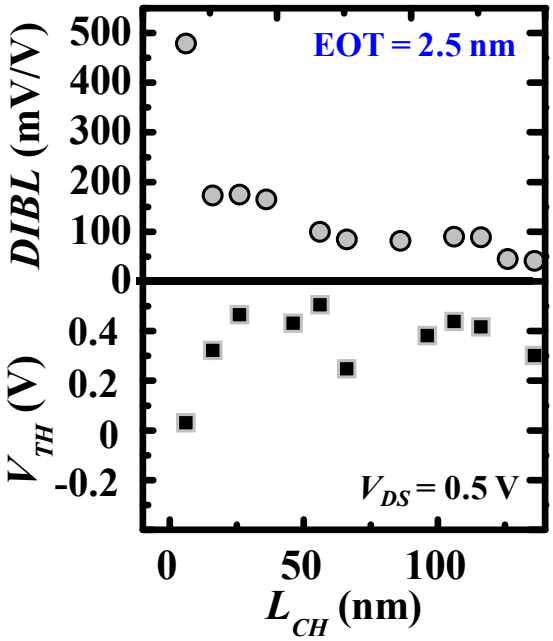


Fig. 2.11 Plot of V_T and *DIBL* versus L_{CH}. Good SCEs control was achieved for L_{CH} down to sub-20nm L_{CH}. The EOT of the devices is 2.5 nm.

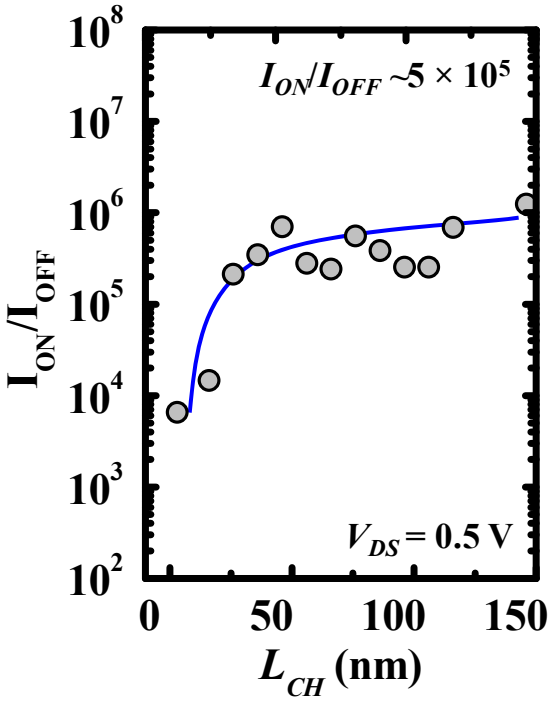


Fig. 2.12 Plot of I_{ON}/I_{OFF} versus L_{CH} for V_D = 0.5 V. Good I_{ON}/I_{OFF} of ~ 5 × 10^5 order was achieved down to sub-20 nm L_{CH}.

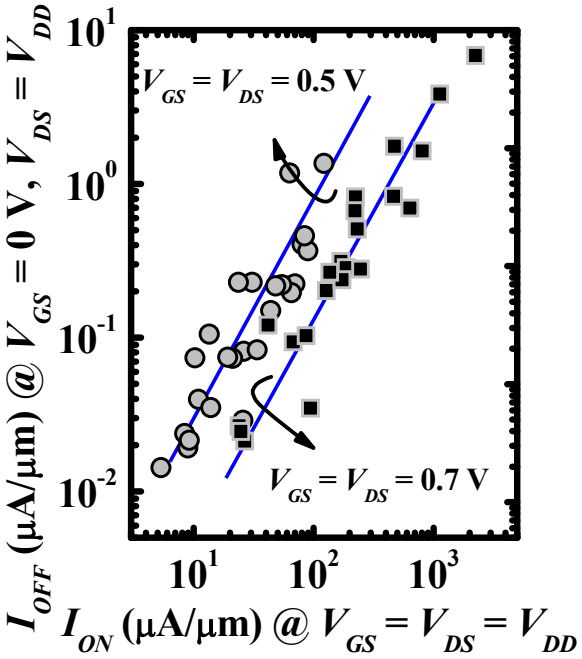


Fig. 2.13 Plot of $|I_{OFF}|$ ($V_G = 0$ V, $V_D = V_{DD}$) versus $|I_{ON}|$ ($V_G = V_D = V_{DD}$) for $V_{DD} = 0.5$V and 0.7 V.

2.5 Investigation of Ballistic Transport in InP/$In_{0.53}Ga_{0.47}As$/InP JLFETs

2.5.1 Transport Analysis of the Short Channel Transistors

Carrier transport analysis of short channel transistors was carried out using the method proposed in [79] which is based on analysis of the channel length dependence of apparent mobility (μ_{app}) and virtual-source (VS) velocity (v_{x0}) [87]-[89]. Since the method does not assume any temperature dependence of transport parameters or any theoretical knowledge of band structure parameters, it can be applied to our short-channel transistors with InP/$In_{0.53}Ga_{0.47}As$/InP BCH.

The VS model requires 6 device parameters including L_{CH}, $I_{OFF,}$ total resistance (R_T), gate capacitance in strong inversion (C_{inv}), subthreshold-swing (*SS*), and drain-induced barrier lowering (*DIBL*). All of them can be obtained directly from experimental data. C_{inv} of 1.65 μF/cm^2 was obtained from the capacitance-voltage (*C-V*) measurement of the long channel

device with L_{CH} of 20 μm. The VS charge density fitting parameter (α) of 3.5 and saturation-transition-region fitting parameter (β) of 1.8 are used for the data fitting using VS model. The VS model assumes a V_G-independent v_{x0} and μ_{app}. This assumption is still valid in our case because our simulated result shows that the v_{ave} variation ($\Delta v_{ave}/v_{ave}$) is less than 10% in the relevant N_S regime, as will be shown later. Meanwhile, we found that μ_{app} variation ($\Delta\mu_{app}/\mu_{app}$) is less than 20 % from the extracted mobility of the long channel devices.

Using the VS model to simultaneously fit I_D-V_G and I_D-V_D data, extrinsic series resistance (R_{ext}) can be extracted, and thus intrinsic values of μ_{app} and v_{x0} can be obtained. Fig. 2.9 (a)-(d) show the measured and fitted I_D-V_G and I_D-V_D curves with two different L_{CH} values. Excellent agreement was obtained over a wide range of bias voltages using V_G independent v_{x0} and μ_{app}.

The extracted v_{x0} and μ_{app} at V_D of 0.5 V versus L_{CH} are shown in Fig. 2.10 (a) and (b), respectively. It can be observed that v_{x0} decreases while μ_{app} increases with increasing L_{CH}. These dependencies will be used to extract the unidirectional thermal velocity (v_{Tx}), critical length (L_C), and mean free path (λ) in the following Section.

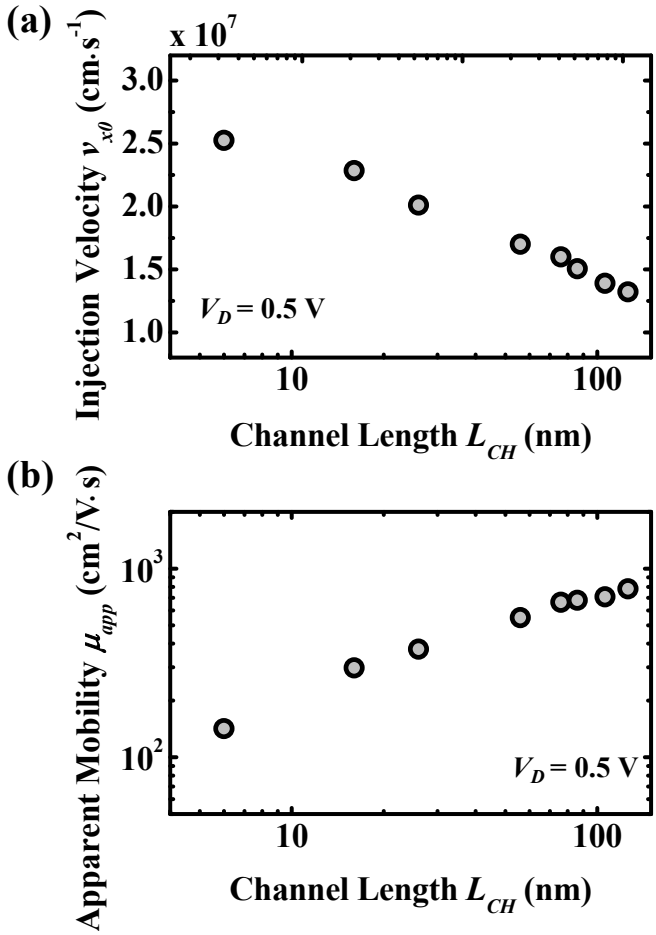


Fig. 2.14 Plot of (a) injection velocity versus channel length (v_{xo}-L_{CH}) and (b) apparent mobility versus channel length (μ_{app}-L_{CH}), extracted using VS model. The v_{xo} increases while μ_{app} decreases with decreasing L_{CH} in our devices, consistent with the reported data in [79]. As the device approaches the ballistic limit, it is expected that v_{x0} approaches the unidirectional thermal velocity (v_{Tx}) while μ_{app} approaches the ballistic mobility (μ_{bal}) which is proportional to L_{CH}.

2.5.2 Extraction of Short-Channel Devices' Ballistic Parameters

The key equations used to extract v_{Tx}, L_C, and λ are summarized as follows [79]

$$\frac{1}{\lambda_{LIN}} = \frac{qv_{Tx}}{2kT}\frac{1}{\mu_{app}} - \frac{1}{L_{CH}}, \tag{2.5}$$

while

$$\frac{1}{\lambda_{SAT}} = \frac{1}{2L_C}\left(\frac{v_{Tx}}{v_{x0}} - 1\right). \tag{2.6}$$

where k is the Boltzman constant, T is the absolute temperature, λ_{LIN} is mean free path in the linear-regime, and λ_{SAT} is the mean free path in the saturation-regime. Assuming $\lambda_{LIN} = \lambda_{SAT}$, we have

$$\frac{L_{CH}}{\mu_{app}} = \frac{kT}{q}\frac{L_{CH}}{L_C}\frac{1}{v_{x0}} + \frac{kT}{qv_{Tx}}\left(2 - \frac{L_{CH}}{L_C}\right). \tag{2.7}$$

Fig. 2.15 (a) plots L_{CH}/μ_{app} versus $1/v_{x0}$ for devices with different L_{CH}. The points follow a straight fitted line. From the slope (s) of the fitted line and intercept (i) with the Y axis, v_{Tx} can thus be extracted based on equation (2.7) and is given by

$$v_{Tx} = \frac{2kT/q - s}{i} = 3.03\times10^7 \text{ cm}\cdot\text{s}^{-1}, \tag{2.8}$$

while L_C can be extracted by

$$L_C = \frac{kT}{q}\frac{1}{s}L_{CH} \approx 0.1 \times L_{CH}. \tag{2.9}$$

Using the extracted v_{Tx} value, the ballistic ratio ($B_{SAT} = v_{x0}/v_{Tx}$) at the saturation regime (V_D = 0.5 V) for our short-channel devices can be obtained as a function of L_{CH}, as shown in Fig. 2.15 (b). B_{SAT} increases with decreasing L_{CH}. The device with the shortest L_{CH} of 6 nm shows B_{SAT} of ~0.75.

Fig. 2.15 (c) plots the extracted λ_{LIN} and λ_{SAT} using equation (3) and (4). Our extracted λ_{LIN} and λ_{SAT} values are in the range of 7-14 nm which is ~1.5 times larger than the λ reported in

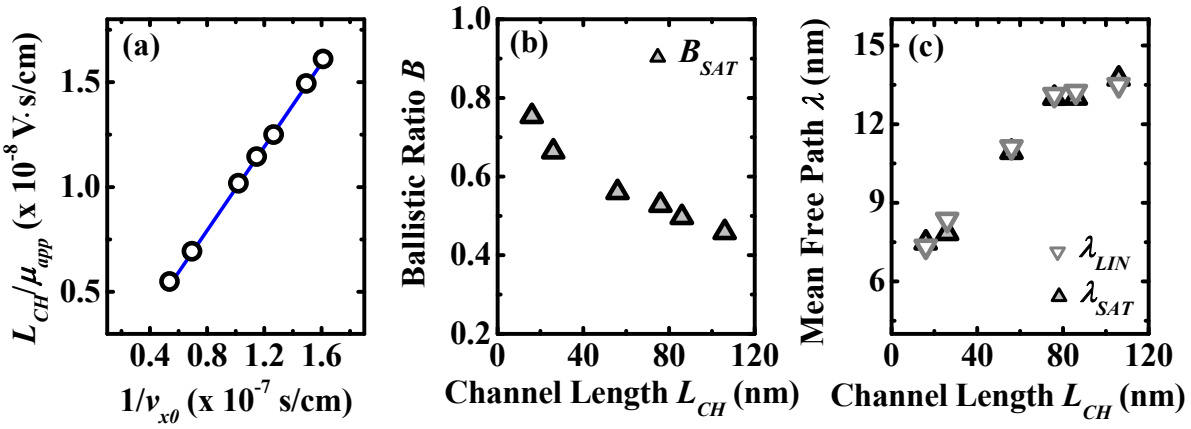


Fig. 2.15 (a) L_{CH}/μ_{app} versus $1/v_{x0}$ plot for devices with InP/$In_{0.53}Ga_{0.47}As$/InP BCH. A straight line through the data points was obtained. (b) Plot of ballistic ratio at saturation regime (B_{SAT}) versus L_{CH}. The device with 6 nm L_{CH} was found to have B_{SAT} of 0.75. (c) Plot of extracted values of λ_{LIN} and λ_{SAT} versus L_{CH}. λ_{LIN} and λ_{SAT} were extracted using equation (2.5) and (2.6), respectively.

[90] for $In_{0.53}Ga_{0.47}As$ short channel nFinFETs. Similar to the observation in [79], our extracted mean free path decreases with decreasing L_{CH}. This phenomenon can be attributed to the momentum transfer between carriers and the plasmon near the source of the short-channel devices [91], [92].

Finally, we compare v_{x0} of the InP/$In_{0.53}Ga_{0.47}As$/InP BCH devices with Si nFETs [79], [93] with L_{CH} ranging from 6 to 200 nm in Fig. 2.16. The stars represent data extracted from this work and with V_D of 0.5 V. As compared with ITRS projected value for strained Si nFETs at V_D = 0.8 V, ~ 30% improvement in v_{x0} was achieved in our devices for L_{CH} less than 10 nm.

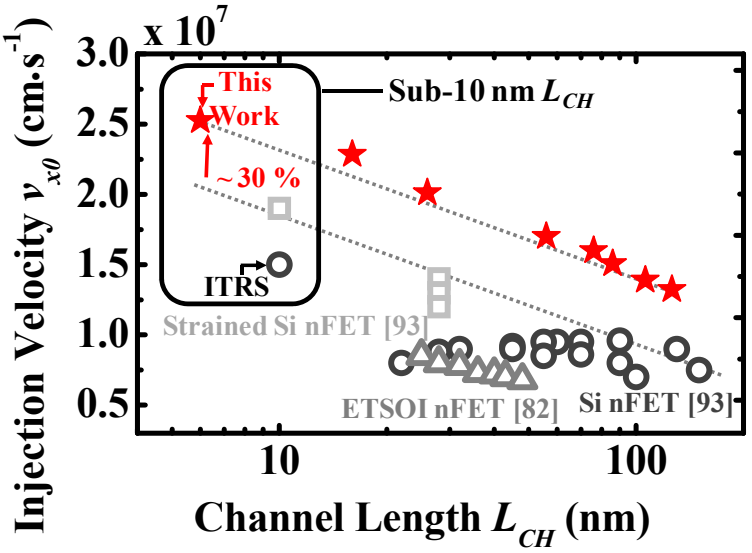


Fig. 2.16 Benchmark plot comparing the v_{x0} of our devices extracted at V_D of 0.5 V with v_{x0} of the state-of-art Si nFETs with V_D ranging from 0.8-1.1V reported in the literature. Strained Si nFETs (square) had been demonstrated with higher v_{x0} over Si nFETs (circle). Our devices (star) shows 30 % higher v_{x0} compared to the ITRS projected v_{x0} values for strained Si nFETs at sub-10 nm L_{CH} regime.

2.6 Summary

In this Chapter, an approach to improve the DOS of $In_{0.53}Ga_{0.47}As$ channel MOSFETs using the InP/$In_{0.53}Ga_{0.47}As$/InP BCH is presented. The DOS of InP/$In_{0.53}Ga_{0.47}As$/InP heterostructure can be improved by engineering the subband energy separation in the Γ-valley. The ballistic transport performance of the InP/$In_{0.53}Ga_{0.47}As$/InP heterostructure with different T_{InGaAs} was studied using semi classical top-of-barrier model. The device with 1 nm T_{InGaAs} was found to provide the highest drive current among the simulated structures, outperforming both InP and $In_{0.53}Ga_{0.47}As$ single channel material at equivalent oxide thickness (EOT) of 0.5 nm. Transistors featuring InP(1 nm)/$In_{0.53}Ga_{0.47}As$(1 nm)/InP heterostructure and channel length (L_{CH}) down to 6 nm were subsequently realized and their short channel transport parameters including v_{Tx}, L_C, and λ were extracted. The shortest device with L_{CH} of 6 nm was found to have

B_{SAT} of 0.75 and the extracted v_{x0} surpasses that of strained Si nFETs by 30% in sub-10 nm L_{CH} regime.

Chapter 3

Towards High Mobility III-V/Ge FinFET CMOS Integrated on Si Platform: Growth and Physical Modeling of $In_xGa_{1-x}As$ (x = 0 and 0.2) on Ge Fin

3.1 Introduction

High-mobility III-V compound semiconductors such as gallium arsenide (GaAs) or indium gallium arsenide (InGaAs) are promising alternative channel material candidates to replace Si in metal-oxide-semiconductor field-effect-transistors (MOSFETs) for high-speed and low-power logic applications [94]-[96]. In Chapter 2, InGaAs nFET with shortest channel length of 6 nm was demonstrated with 30 % higher injection velocity as compared to Si at sub-10 nm technology node. However, the device was realized on InP substrate, which is costly and difficult to make in large wafer size. In order to reduce the cost of production and achieve high volume production, III-V materials have to be integrated on silicon substrates to leverage on their mature Si complementary-metal-oxide semiconductor (CMOS) fabrication technology and infrastructure.

Intensive research has been carried out to integrate III-V material such as GaAs on Si. This includes direct growth of GaAs on Si islands [97], flip-chip bonding [98],[99], insertion of a silicon-germanium (SiGe) graded buffer layer for GaAs growth [100],[101], and selective aspect ratio trapping (ART) method [102]. Nanoheteroepitaxy of GaAs on Ge fins [103],[104] is another promising integration scheme that could enable co-integration of III-V (GaAs) n-channel

field- effect-transistor (nFET) and Ge p-channel field-effect-transistor (pFET) on a Si platform. However, there are many challenges for GaAs growth on Ge, such as the formation of antiphase domains (APDs) that typically occurs during the growth of polar III-V materials on non-polar materials. APDs can be effectively suppressed with the use of offcut substrates [105]-[106]. We performed initial work on the selective growth of GaAs on Ge fins or stripes with different in-plane orientations formed on a Germanium-on-Insulator (GeOI) wafer having an offcut (001) Ge surface [107]. The GaAs crystals grown on Ge fins have shapes that depend on the fin orientations.

In this Chapter, we report a physical model to explain the effect of Ge fin orientation on the facet angles of GaAs crystals grown on the Ge fins with different in-plane orientations formed on a GeOI wafer having an offcut (001) Ge surface. The understanding of the as-grown GaAs surface orientation is critical for the design of high performance metal-oxide-semiconductor (MOS) devices, since the surface orientation can affect the interface state density (D_{it}), surface roughness scattering, and electron mobility [108]-[109]. In the second part of this Chapter, selective growth of $In_{0.2}Ga_{0.8}As$ on Ge fin is demonstrated. The growth mechanism of $In_{0.2}Ga_{0.8}As$ on Ge fin was analyzed through extensive Scanning Electron Microscope (SEM) and Transmission Electron Microscope (TEM) characterizations. Integration of high-quality $In_{0.2}Ga_{0.8}As$ on Ge fin could enable the realization of high mobility InGaAs n-FinFET and Ge p-FinFET complementary-metal-oxide-semiconductor (CMOS) on Si platform for future low power and high performance logic applications.

3.2 Nanoheteroepitaxy of Gallium Arsenide (GaAs) on Germanium (Ge) Fins

A schematic showing our experimental setup is presented in Fig. 3.1. A GeOI wafer with 50 nm-thick Ge on 100 nm-thick SiO_2 (buried oxide or BOX) on Si was used as the starting substrate. The Ge surface has an (0 0 1) offcut surface with the offcut oriented 10° towards the <1 1 1> direction, i.e. the normal to the surface is $[8\ \bar{1}\ 1]$. 20 nm of SiO_2 was initially deposited as a hardmask. Electron Beam Lithography (EBL) was used to define photoresist patterns on the SiO_2 hardmask. Lines with various angles θ with respect to the <0 1 1> flat were defined. θ ranges from 25° to 70°. This was followed by dry etching and hardmask removal. Rapid Thermal Oxidation (RTO) at 400 °C for 60 s was then used to smoothen the sidewalls of the fins.

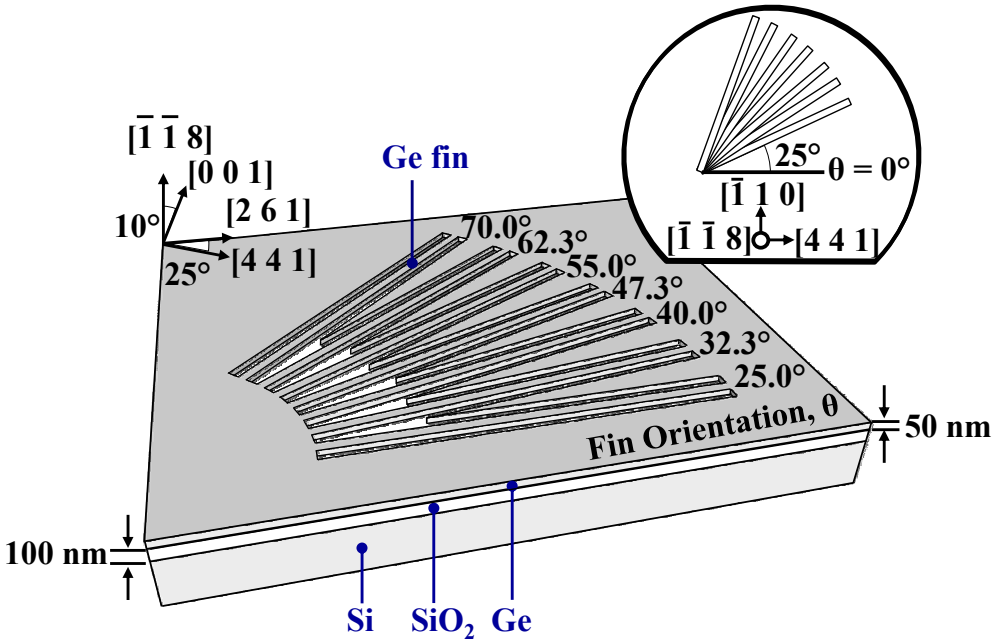


Fig. 3.1 Fins with different orientations (θ = 25° to 70°) defined on a GeOI substrate having an offcut (0 0 1) surface with the offcut oriented 10° towards the <1 1 1> direction.

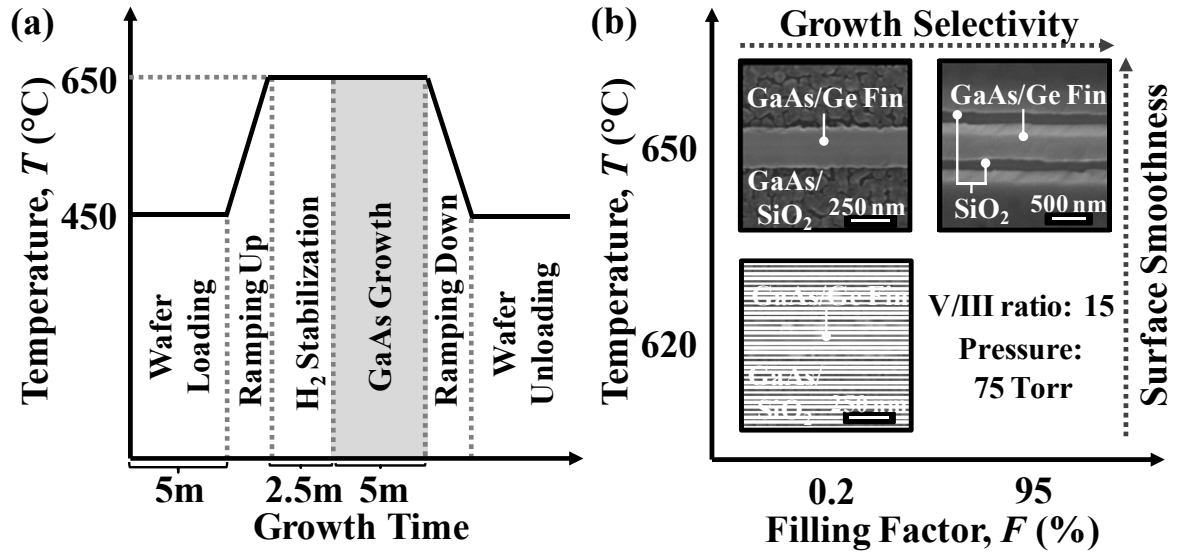


Fig. 3.2 (a) Key growth sequence for selective growth of GaAs on Ge fins. (b) Growth splits involving temperature and filling factor for optimizing the growth of GaAs on Ge fins. The V/III ratio and growth pressure are maintained at 15 and 75 Torr, respectively. Growth selectivity can be improved with larger filling factor while the surface roughness can be improved with higher growth temperature.

Next, the sample was cleaned using a cyclic DHF ($HF:H_2O=1:50$) treatment before being loaded into an AIXTRON 200 MOCVD tool for GaAs growth for 600 s at a temperature of 650 °C and a pressure of 75 Torr. The III-V precursors used were TributhylArsenic (TBAs) and TrimethylGallium (TMGa). The ratio of the flow rate (measured in sccm) of TMGa to that of TBAs is 15:1 [110]. The GaAs growth sequence is illustrated in Fig 3.2 (a). The GeOI sample first went through pre-bake at 420 °C for 5 minutes, followed by 2.5 minutes high temperature (650 °C) stabilization in H_2 ambient. Then GaAs growth was performed for 5 minutes. The growth conditions were optimized by varying the growth temperature and filling factor as shown in Fig. 3.2 (b). Good growth selectivity and smooth surface for as-grown GaAs on GeOI sample was achieved with 95 % filling factor at growth temperature of 650 °C. All the MOCVD growth processes in this Chapter were performed by Y. Cheng from Institute of Materials Research and Engineering (IMRE).

Fig 3.3 (a) shows High Resolution X-Ray Diffraction (HR-XRD) (004) spectra of the ω-2θ scan of GeOI samples after GaAs growth. The separation of the Ge and GaAs peak exhibits a larger value over 0.1° as compared with the theoretical prediction of about 0.05°. This is due to the fact that GaAs deposited on the mis-oriented Ge substrate usually creates a tilt angle between the lattice plane of the substrate and the epitaxial layer, resulting in the displacement of the epitaxial layer peak in the diffraction curve [111]. Top view inspection of the Ge fin before and after the growth of GaAs on Ge fins was performed using SEM, as shown in Fig. 3.3 (b). A cross-section TEM image was taken along line A-A` in Fig. 3.3 (b) to examine the structure of the as-grown GaAs on the Ge fins. Faceted surfaces of the as-grown GaAs were observed in the TEM image in Fig. 3.3 (c).

The left facet makes an angle α with respect to the Ge surface plane, and the right facet makes an angle β with respect to the Ge surface plane. These facets correspond to the slowest growing planes. In general, the left and right facets are not symmetrical and are not equivalent crystal planes. It should be noted that the facet angles α and β are defined in a plane perpendicular to the longitudinal axis of each fin, henceforth referred to as fin cross-section plane. Fig. 3.3 (d) illustrates a three-dimensional schematic of the GaAs grown on a fin with orientation θ. It should also be noted that the TEM plane which cuts along line A-A` is a $(10\ \bar{4}5\ 127)$ plane and is not generally the fin cross-section plane. In the TEM plane, the left and the right facet angles are $\alpha$` and β`, respectively. By simple geometry, we have

$$\tan(\alpha) = \frac{\tan(\alpha`)}{\cos(\theta)}, \tag{3.1}$$

and

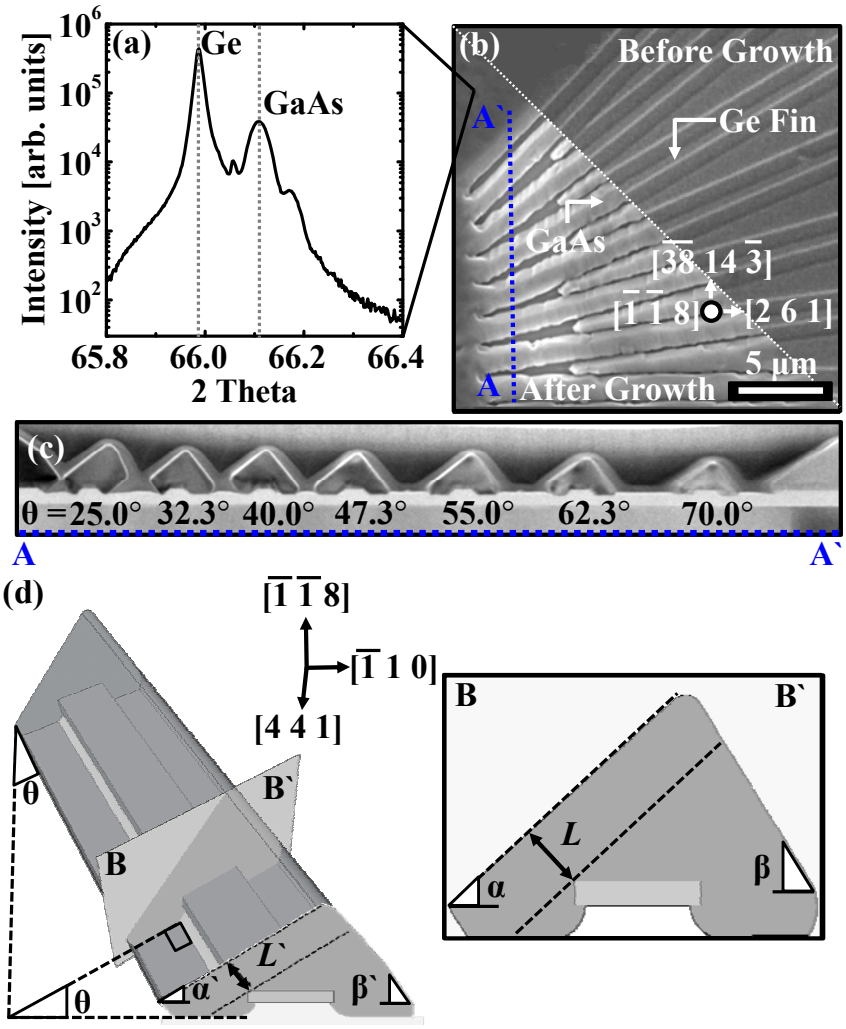


Fig. 3.3 (a) High resolution XRD showing distinct Ge and GaAs peaks. SEM images of (b) Ge fins before and after GaAs growth. (c) Cross-sectional TEM image (bright-field) along the line A-A` in (b) shows the faceted growth of GaAs on Ge fins. (d) Schematic showing the method for extracting the growth rate in a direction perpendicular to the facet plane. The growth rate is proportional to *L* or *L'*.

$$\tan(\beta) = \frac{\tan(\beta')}{\cos(\theta)}. \tag{3.2}$$

The growth rate in a direction perpendicular to a GaAs facet on Ge fin is proportional to the perpendicular distance *L* of the GaAs facet plane to the nearest Ge fin corner. This is illustrated in Fig. 3.3 (d) where the cross-section is along B-B` of the fin. In the TEM plane, the

perpendicular distance between the GaAs facet and the nearest Ge fin corner is denoted as L`. $L$ can be obtained from the projection of $L$` onto the fin cross-section plane using

$$L = L`\cos(\theta)\frac{\sin(\alpha)}{\sin(\alpha`)}, \tag{3.3}$$

for the left GaAs facet and

$$L = L`\cos(\theta)\frac{\sin(\beta)}{\sin(\beta`)}, \tag{3.4}$$

for the right GaAs facet.

The growth rate in a direction perpendicular to a slow-growing GaAs facet or plane can therefore be obtained by

$$r = \frac{L}{t}, \tag{3.5}$$

where the growth time t in our experiment is 600 s.

High Resolution TEM (HRTEM) images (bright-field) were taken at the GaAs-Ge interface at the top and side of a fin (Fig. 3.4) and they reveal good crystalline quality. No crystalline defects were observed. The zone axis (ZA) for the HRTEM is [010].

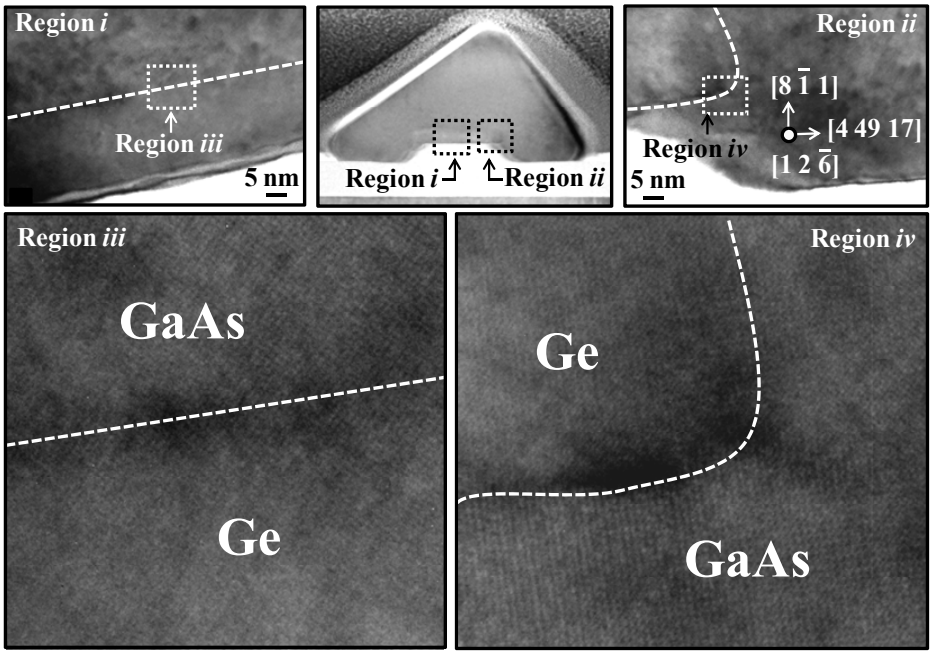


Fig. 3.4 HRTEM (bright-field) confirms the good crystalline quality of the GaAs grown on the Ge fins. Zoomed-in views of the interface between GaAs and Ge at the top and side of the fin are also shown. The zone-axis (ZA) of the TEM is [010]. The TEM is performed at Institute of Materials Research and Engineering (IMRE) through a service contract.

Facet angles α and β and their corresponding growth rates r were extracted from TEM image for each fin orientation and are presented in Table 2.1. It is interesting to note that there is a decreasing trend for the growth rate with increasing fin orientation from $\theta = 25°$ to $\theta = 70°$. On the other hand, the facet angles α and β increase with increasing fin orientation from $\theta = 25°$ to $\theta = 70°$. These observed growth rates for the left GaAs facets are plotted as vectors in a three-dimensional space in Fig. 3.5. Each vector corresponds to the growth rate in a direction corresponding to a GaAs facet in the fin cross-section plane.

Table 3.1 Experimental facet angles α and β, and growth rate r extracted from each fin orientation.

Fin Orientation θ (°)	**Facet Angle** α (°)	**Growth Rate r (nm/s)**	**Facet Angle** β (°)	**Growth Rate** r **(nm/s)**
25.0	38.0	90	48.1	234
32.3	38.6	101	51.7	151
40.0	39.4	113	50.8	123
47.3	39.8	113	52.0	106
55.0	41.9	87	54.1	98
62.3	43.4	94	57.2	87
70.0	46.1	86	61.3	83

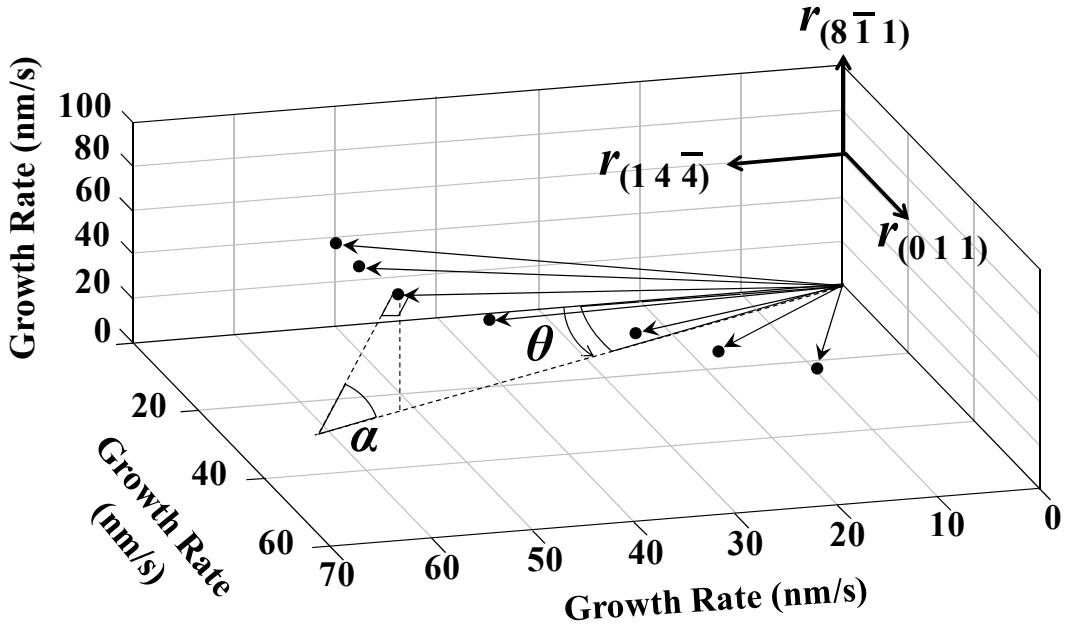


Fig. 3.5 Experimental growth rates of the left facet of as-grown GaAs on Ge fin for various fin orientations plotted as vectors in three-dimensional growth rate space.

3.3 Physical Modeling of GaAs Growth on Ge Fins

3.3.1 GaAs Facet Identification

The GaAs facets formed on Ge fins with various orientations are investigated next using a model based on Wulff's theory [112]. According to the Wulff theory, the shape of an as-grown crystal structure on a convex shaped surface can be constructed by intersections of all the growth facet planes which are displaced from a reference point by a perpendicular distance proportional to their growth rate. The smallest shape confined by intersection of all the growth facet planes predicts the shape of the crystal grown. In other words, growth facets on a convex surface tend to be dominated by the slowest growing facets [113]. For example, GaAs which is grown on an infinitesimally small seed or GaAs nanoparticle would result in an Equilibrium Crystal Shape (ECS) [114]-[115] that terminates with {1 1 0}, {1 1 1}A and {1 1 1}B surfaces, which are the slowest growing facets. In the case where the growth seed is prepared on an offcut substrate such as a GeOI (1 0 0) substrate with a 10° offcut towards <1 1 1>, the resulting ECS would be tilted towards [1 1 1] with the substrate's normal vector [8 $\bar{1}$ 1] making an angle of 10^{o} with respect to the ECS [1 0 0] vector as shown in Fig. 3.6 (a).

We note that a cross-section obtained by intersection of an arbitrary plane with the ECS and passing through the ECS center would yield a shape circumscribed by the slowest growing planes. A fin structure can be constructed as shown in Fig. 3.6 (b). The resulting fins are our predicted final fin structures since they have cross-sections that intersect with the slowest growing facets of the ECS.

In our experiment, the Ge fins are prepared on the $(8\ \bar{1}\ 1)$ plane and the fin orientation θ = 0° is defined along the $<1\ 4\ \bar{4}>$ direction. Thus, the fin cross-section plane for θ = 0°

intersects with the ECS on the (0 1 1) plane as shown in Fig. 3.6 (b). Similarly, the fin cross-section plane for $\theta = 90°$ intersects with the ECS on the $(1\ 4\ \bar{4})$ plane. In general, the cross-section for a θ-oriented fin can be predicted by the intersection of the fin cross-section plane [that makes a counter-clockwise angle θ with the (0 1 1) plane] with the ECS.

Facet angles α and β shown in the ECS cross-section in Fig. 3.6 (b) correspond to the GaAs facet angles defined earlier in the fin cross-section plane in Fig. 3.3 (d). Since α and β are related to the ECS, they can be modeled as a function of fin orientation θ with the known ECS facet angles as well as the substrate offcut angle, φ.

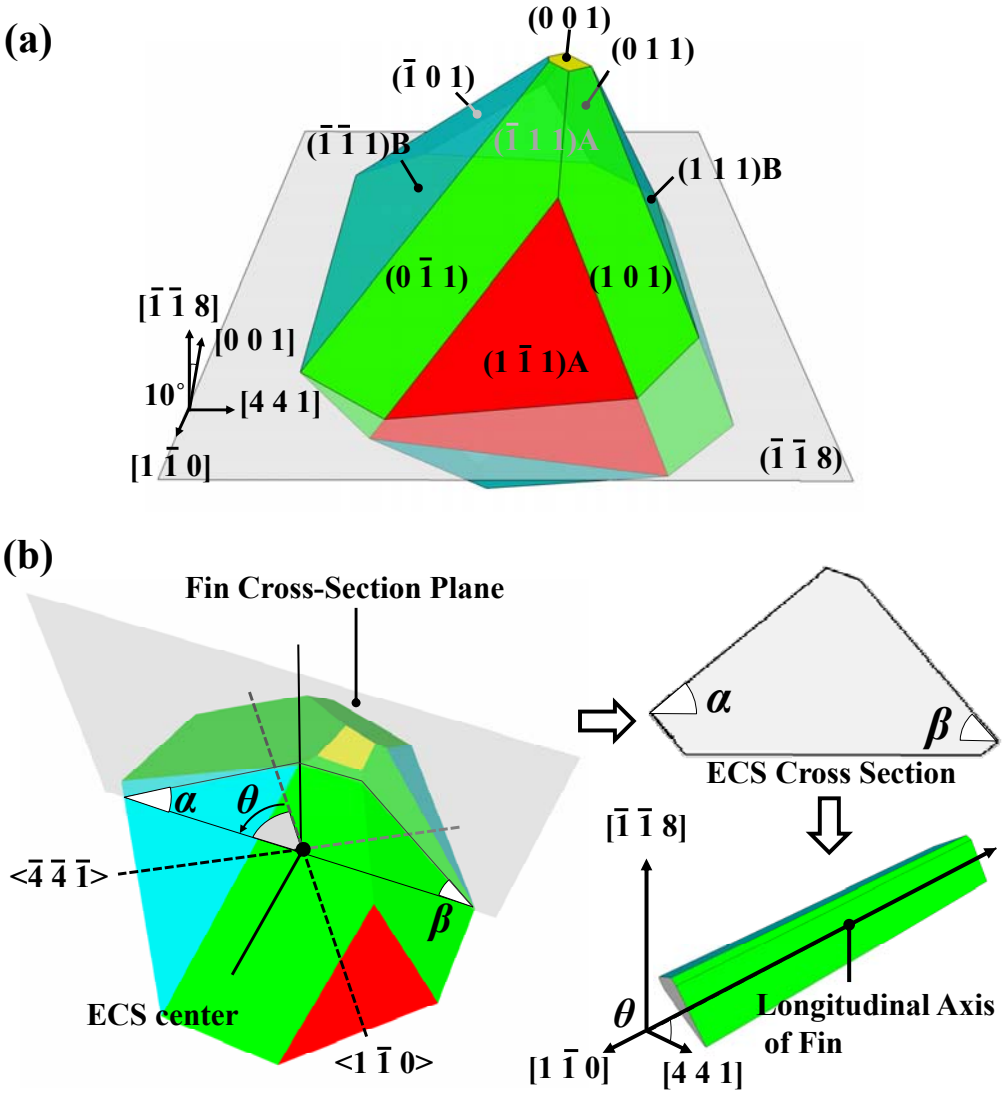


Fig. 3.6 (a) Equilibrium Crystal Shape (ECS) showing the facets formed when growth is performed on an infinitesimally small seed on a 10° offcut substrate. The slowest growing facets are {1 1 0}, {1 1 1}A and {1 1 1}B. (b) ECS cross-sections can be used to predict the as-grown GaAs facets on Ge fins with various fin orientation θ by repeating the ECS cross-section along its normal vector direction.

The facet angles α and β for various intersecting ECS facets can thus be derived as:

{1 1 1}A:

$$\alpha(\theta,\varphi) = \tan^{-1}[\frac{\tan(54.7^\circ)}{\cos(\varphi)}]\cos\{\tan^{-1}[\frac{\tan(\theta)}{\cos(\varphi)}]\} - \tan^{-1}[\tan(\varphi)\sin(\theta)], \quad (3.6)$$

$$\beta(\theta,\varphi) = \tan^{-1}[\frac{\tan(54.7^\circ)}{\cos(\varphi)}]\cos\{\tan^{-1}[\frac{\tan(\theta)}{\cos(\varphi)}]\} + \tan^{-1}[\tan(\varphi)\sin(\theta)], \quad (3.7)$$

{1 1 0}:

$$\alpha(\theta,\varphi) = \tan^{-1}[\frac{\tan(45^\circ)}{\cos\{\tan^{-1}[\tan(\varphi)\sin(45^\circ)]\}|}\cos(|45^\circ - \theta|)] - \tan^{-1}[\tan(\varphi)\sin(\theta)], \quad (3.8)$$

$$\beta(\theta,\varphi) = \tan^{-1}[\frac{\tan(45^\circ)}{\cos\{\tan^{-1}[\tan(\varphi)\sin(45^\circ)]\}}\cos(|45^\circ - \theta|)] + \tan^{-1}[\tan(\varphi)\sin(\theta)], \quad (3.9)$$

{1 1 1}B:

$$\alpha(\theta,\varphi) = \tan^{-1}[\frac{\tan(54.7^\circ)}{\cos(\varphi)}\cos\{\tan^{-1}[\frac{\cos(\varphi)}{\tan(\theta)}]\}] - \tan^{-1}[\tan(\varphi)\sin(\theta)], \quad (3.10)$$

$$\beta(\theta,\varphi) = \tan^{-1}[\frac{\tan(54.7^\circ)}{\cos(\varphi)}\cos\{\tan^{-1}[\frac{\cos(\varphi)}{\tan(\theta)}]\}] + \tan^{-1}[\tan(\varphi)\sin(\theta)], \quad (3.11)$$

where φ is 10° in our experiment. The values 54.7° and 45° are the angles made by {1 1 1} and {1 1 0} planes, respectively with respect to {1 0 0} plane.

The ECS facets that are intersected by the fin cross-sections can be identified by comparing the experimentally extracted facet angles from Table 2.1 with the modeled facet angles using Equations (6) to (11) as shown in Fig. 3.7. The comparison shows a good fit between the modeled and experimentally extracted α and β. The cross-sections of fins oriented from θ = 25° to θ = 40° intersect with the {1 1 0} ECS facet, while the cross-sections of fins oriented from θ = 47.3° to θ = 70° intersect with the {1 1 1}B ECS facet.

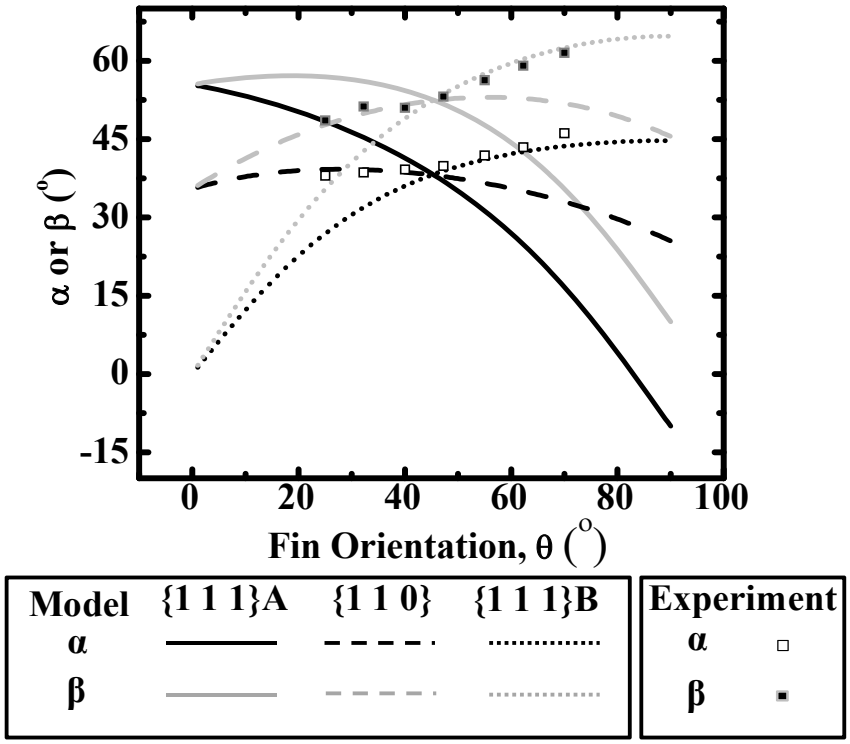


Fig. 3.7 Facet angles α and β plotted as a function of fin orientation. Extracted angles from TEM are plotted as symbols, and calculated angles are plotted as lines. The experimental facet angles fit well with the calculated curves for α and β.

3.3.2 Calculation of Growth Rates for Equilibrium Crystal Structure (ECS) Facets

The growth rate in a direction perpendicular to a plane (m n o) is proportional the shortest perpendicular distance from the ECS facet plane to the ECS center. The shortest perpendicular distance corresponds to the growth thickness $L_{\{m\ n\ o\}}$ of that particular plane. The growth thicknesses of the slowest growing facets of the ECS are denoted as $L_{\{8\ 1\ 1\}}$ $L_{\{1\ 1\ 1\}A}$, $L_{\{1\ 1\ 0\}}$ and $L_{\{1\ 1\ 1\}B}$ as shown in Fig. 3.8 (a).

The growth thickness of the ECS facet in the direction normal to the GeOI substrate, $L_{\{8\ 1\ 1\}}$, can be extracted directly from the thickness of the as-grown GaAs on the un-patterned GeOI bulk region. However, the growth thicknesses of the slowest growing facets of the ECS [$L_{\{1\ 1}$

$_{1\}A}$, $L_{\{1\ 1\ 0\}}$ and $L_{\{1\ 1\ 1\}B}$] cannot be measured directly from the experimental GaAs facet growth thickness L. This is because the experimental GaAs facet growth thickness L is not always the shortest growth thickness measured from the ECS facet plane to the ECS center.

Fig. 3.8 (b) shows a schematic of the ECS which is projected onto the (8 $\bar{1}$ 1) plane. The projection outlines the intersects of various ECS facets with the (8 $\bar{1}$ 1) plane. Perpendicular lines connecting these boundaries to the ECS center make specific angles γ with respect to the <0 1 1> direction. These perpendicular lines correspond to the ECS-intersecting plane that contains the shortest vector from the ECS facet plane to the ECS center. In order to compute the growth thicknesses of the slowest growing planes of the ECS [$L_{\{1\ 1\ 1\}A}$, $L_{\{1\ 1\ 0\}}$ and $L_{\{1\ 1\ 1\}}$], each experimental growth thickness L for various fin orientations was first associated with their respective intersecting ECS facets. This was done previously in Section A. Subsequently, each experimental growth thickness L can be projected onto the ECS-intersecting plane that contains the shortest vector from the ECS facet plane to the ECS center to compute its corresponding ECS facet growth thickness as follows:

ECS growth thickness calculation for the left half of the ECS uses

$$L_{\{1\ 1\ 1\}A} = \frac{L\cos(\theta-\gamma)\sin[\alpha(\gamma,\ \varphi)]}{\sin(\alpha)}, \tag{3.12}$$

$$L_{\{1\ 1\ 0\}} = \frac{L\cos(|\theta-\gamma|)\sin[\alpha(\gamma,\ \varphi)]}{\sin(\alpha)}, \tag{3.13}$$

$$L_{\{1\ 1\ 1\}B} = L\frac{\cos(\gamma-\theta)\sin[\alpha(\gamma,\ \varphi)]}{\sin(\alpha)}, \tag{3.14}$$

where $\alpha(\gamma, \varphi)$ takes the same form as in Equations (6), (8) and (10). The value of γ for {1 1 1}A, {1 1 0} and {1 1 1}B are -7°, 53°, and 90°, respectively.

ECS growth thickness calculation for the right half of the ECS uses

$$L_{\{1\ 1\ 1\}A} = \frac{L\cos(|\theta-\gamma|)\sin[\beta(\gamma,\ \varphi)]}{\sin(\beta)}, \tag{3.15}$$

$$L_{\{1\ 1\ 0\}} = \frac{L\cos(|\theta-\gamma|)\sin[\beta(\gamma,\ \varphi)]}{\sin(\beta)}, \tag{3.16}$$

$$L_{\{1\ 1\ 1\}B} = \frac{L\cos(\gamma-\theta)\sin[\beta(\gamma,\ \varphi)]}{\sin(\beta)}, \tag{3.17}$$

where $\beta(\gamma, \varphi)$ takes the same form as in Equations (7), (9) and (11). The value of γ for {1 1 1}A, {1 1 0} and {1 1 1}B in this case are 7°, 51°, and 90°, respectively. Note that α and β in the denominator in Equations (3.12) to (3.17) are the experimentally obtained values.

ECS facet growth rate can thus be determined from the calculated growth thickness using

$$r_{\{m\ n\ o\}} = \frac{L_{\{m\ n\ o\}}}{t}. \tag{3.18}$$

The growth rates for each equivalent plane obtained from Equations (3.12) to (3.18) are averaged and plotted as box plots in Fig. 3.9. The ratio of the averaged ECS facet growth rates for {8 1 1}:{1 1 1}A:{1 1 0}:{1 1 1}B is 18.2:11.2:10:9.2.

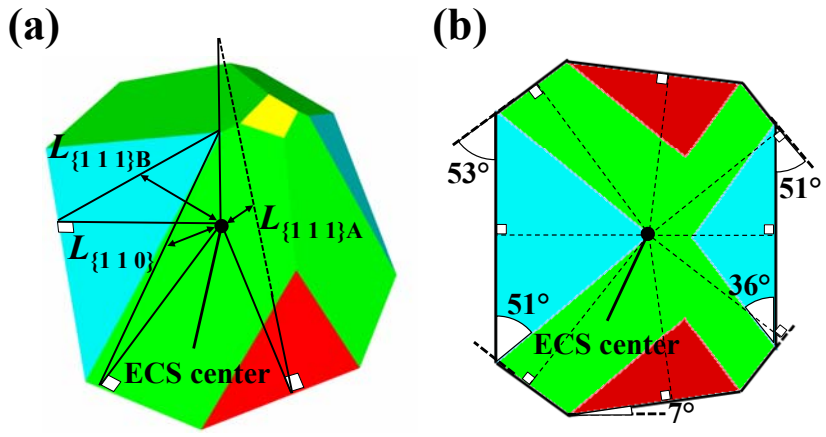


Fig. 3.8 (a) Growth thicknesses of the slowest growing facets of the ECS. (b) Planar projection of the ECS onto the {8 1 1} plane showing the various intersecting ECS boundaries on the $(8\ \bar{1}\ 1)$ plane.

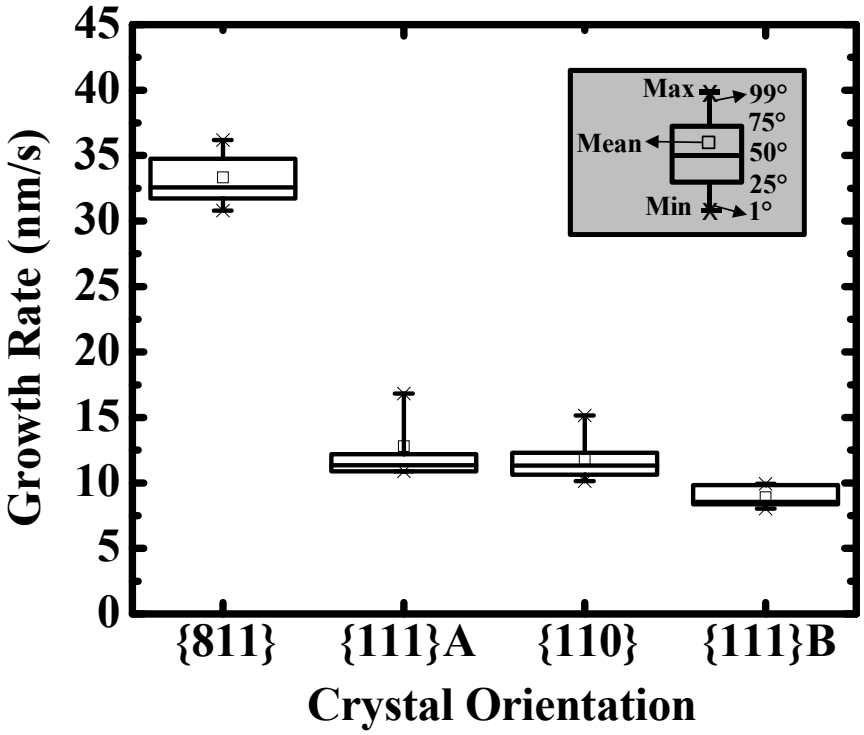


Fig. 3.9 Extracted growth rates of the slowest growing facets of the ECS. Average growth rate ratio for {8 1 1}:{1 1 1}A:{1 1 0}:{1 1 1}B of the ECS is measured to be 18.2:11.2:10:9.2.

From the thermodynamic standpoint, the equilibrium crystal shape (ECS) can be determined by minimization of the free energy of the crystal. Specifically, the planes with lower surface energy are energetically more favorable, and thus dominate the ECS. In the case of Si and Ge, the surface energies of various planes can be explained through broken-bond-counting model per unit area, where higher surface energies planes have higher broken bonds density. Since the broken bond density for Si and Ge increases in the order of (111) < (110) < (001), the surface energies also increases in the order of (111) < (110) < (001) [116].

However for compound semiconductor such as GaAs, the presence of cations (Ga) and anions (As) could also lead to certain polarized surfaces which are thermodynamically unstable. Moll et al. [117] and Platen et al. [118] have calculated the surface energies of the various GaAs planes using first principle density functional theory (DFT). Here, the surface energies of typical

GaAs (001), (110), (111)A, and (111)B planes are briefly discussed. GaAs (110) is the cleavage plane which contain the same number of cations and anions, thus it is intrinsically neutral. Under moderate As growth environment (which can be controlled by adjusting the V/III ratio), the cleavage surface is energetically most favorable as compared to the other polar (001), (111)A and (111)B surfaces. Thus, it is predicted that the GaAs ECS would be defined by the (110) planes. However, in As-rich growth environment which is the case for our experiment, the surface energy of all the planes under discussion are relatively similar with the slight increase in the order of (111)B < (110) [or (001)] < (111)A. This implies that all the planes under discussion could co-exist in the GaAs ECS under As-rich growth environment, as predicted by Moll et al., [117]. Our extracted growth rate in Fig. 3.9 and constructed ECS in Fig. 3.8 are in good agreement with these findings.

Furthermore, in the As-rich growth environment, the (111)B surface undergone As-trimer (2×2) surface reconstruction [117], [119]. It had been reported that this surface could disturb the incorporation of Ga adatom into the lattice sites since there is no Ga-adsorption sites on such surface. Therefore, the migration length of Ga-adatom on (111)B surface increases with increasing III/V ratio. This reduces the growth rate of the (111)B GaAs plane and increases the growth rate of the adjacent planes since the Ga adatom could diffuse and get incorporated in the sites of the other surface planes or get desorbed before incorporation on the (111)B surface. This is consistent with the growth rate as shown in Fig. 3.9.

3.3.3 Prediction of As-Grown GaAs Facets on Different Ge Fins Orientations with Constructed ECS

The ECS for our experiment is obtained by the construction method proposed in Ref. [112] as discussed earlier, with inputs from the growth rates of the slowest growing facets of the ECS computed in Section B. ECS facets are initially drawn as independent planes using three-dimensional software, taking care of the changes in facet angles due to the substrate offcut. Each plane is then displaced with respect to the ECS center along the plane's normal relative to its growth rate. The smallest crystal structure confined by intersection of all the planes defines the ECS for this experiment.

The ECS cross-sections which correspond to fin cross-sections from θ = 25° to 70° are extracted as shown in Fig. 3.10 (a). Each ECS cross-section is then extended along the longitudinal fin axis to construct the GaAs-on-Ge fins as shown in Fig. 3.10 (b). The resulting three-dimensional GaAs-on-Ge fin structures can thus be predicted.

In order to compare with the GaAs facets in the TEM (bright-field) cross-section plane cut along A-A` with zone axis shown in Fig. 3.3 (c), the fin cross-sections were taken along C-C` from the constructed fins as shown in Fig. 3.10 (c). The resulting GaAs cross-sections in the C-C` plane compare well with the experimental results.

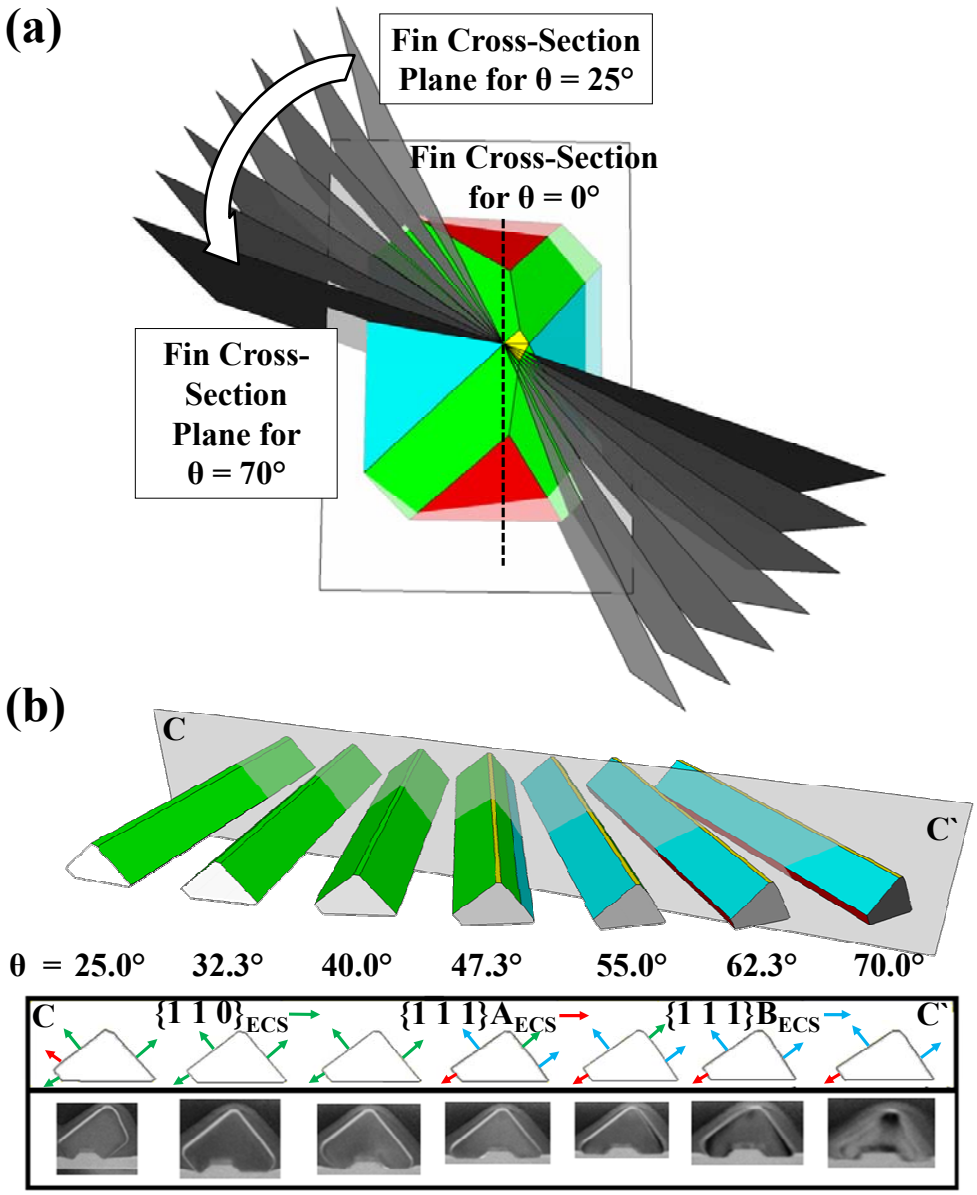


Fig. 3.10 (a) Modeling of GaAs facets formed on Ge fins with various orientations using the ECS constructed from the growth rates extracted from our experiment. Cross-sections of the ECS corresponding to the cross-sections of fins oriented from θ = 25° to θ = 70° are obtained. (b) Resulting ECS cross-sections are used to construct the fins by repeating the cross-sections along their respective fin longitudinal axes. Cross-sections of GaAs facets taken along C-C` are compared with the experimental GaAs facets shown in TEM images (bright-field) along A-A` in Fig. 3.3 (b). The predicted GaAs facets match well with the experimental result. The cross-sections of fins oriented from θ = 25° to θ = 40° intersect with the {1 1 0} ECS facet (denoted by $\{1\ 1\ 0\}_{ECS}$) while cross-sections of fins oriented from θ = 47.3° to θ = 70° intersect with the {1 1 1}B ECS facet (denoted by $\{1\ 1\ 1\}B_{ECS}$).

3.4 Process Development for Nanoheteroepitaxy of Indium Gallium Arsenide ($In_{0.2}Ga_{0.8}As$) on Ge Fins

The Ge fin sample for the growth of $In_{0.2}Ga_{0.8}As$ on Ge fin was prepared in the same way as mentioned in Section 3.2. Before the $In_{0.2}Ga_{0.8}As$ growth, the Ge fins were treated with 10 cycles of cleaning using H_2O and diluted hydrofluoric acid (DHF). The III-V precursors used were TributhylArsenic (TBAs), TrimethylGallium (TMGa), and TrimethylIndium (TMIn). The $In_{0.2}Ga_{0.8}As$ growth sequence illustrated in Fig 3.11 (a) is similar to the GaAs growth sequence in Fig 3.2 (a), where the Ge fin sample first went through pre-bake at 420 °C for 5 minutes, followed by 2.5 minutes high temperature (640 °C) stabilization in H_2 ambient.

Then $In_{0.2}Ga_{0.8}As$ growth was then performed for 4 minutes. The growth conditions were

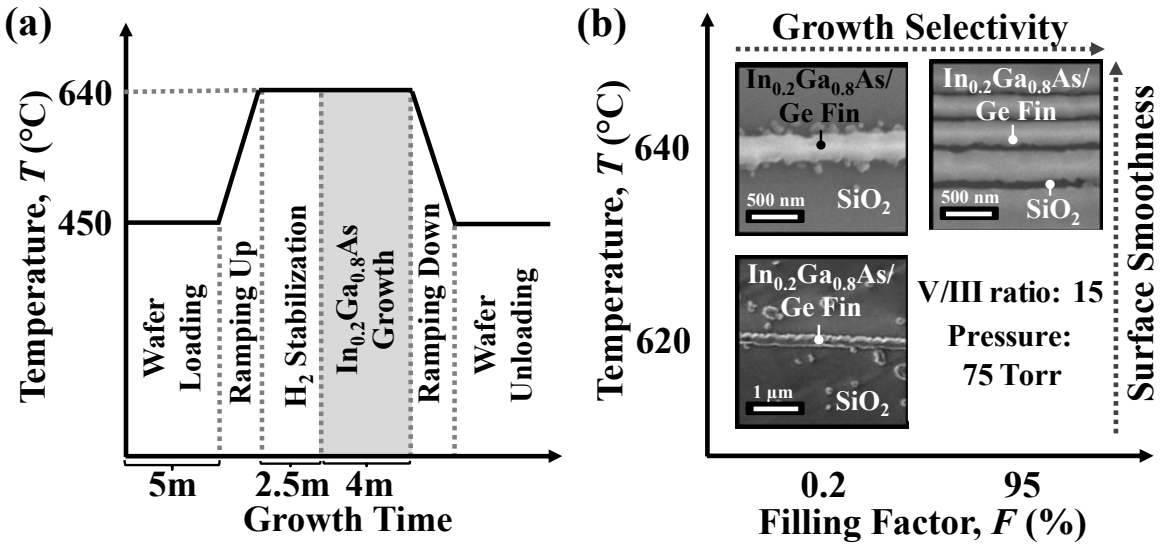


Fig. 3.11 (a) Key growth sequence for selective growth of $In_{0.2}Ga_{0.8}As$ on Ge fins. (b) Growth splits involving temperature and filling factor for optimizing the growth of $In_{0.2}Ga_{0.8}As$ on Ge fins. The V/III ratio and growth pressure are maintained at 15 and 75 Torr, respectively. Growth selectivity can be improved with larger filling factor, *F* while the surface roughness can be improved with higher growth temperature.

optimized by varying the growth temperature and filling factor, as shown in Fig. 3.11 (b). Good growth selectivity and smooth surface for as-grown $In_{0.2}Ga_{0.8}As$ on Ge fin sample were achieved with 95 % filling factor at growth temperature of 640 °C.

The SEM images in Fig. 3.12 (b) and (d) show the selective and continuous growth of $In_{0.2}Ga_{0.8}As$ on Ge fins using the optimized growth temperature at 640 °C. $In_{0.2}Ga_{0.8}As$ grown on narrow Ge fins was found to be faceted, similar to our previously reported results on the physical modeling of the as-grown GaAs facet on Ge fins. Focused ion beam (FIB) cut was performed along the line A-A` in Fig. 3.12 (d) for further TEM analysis.

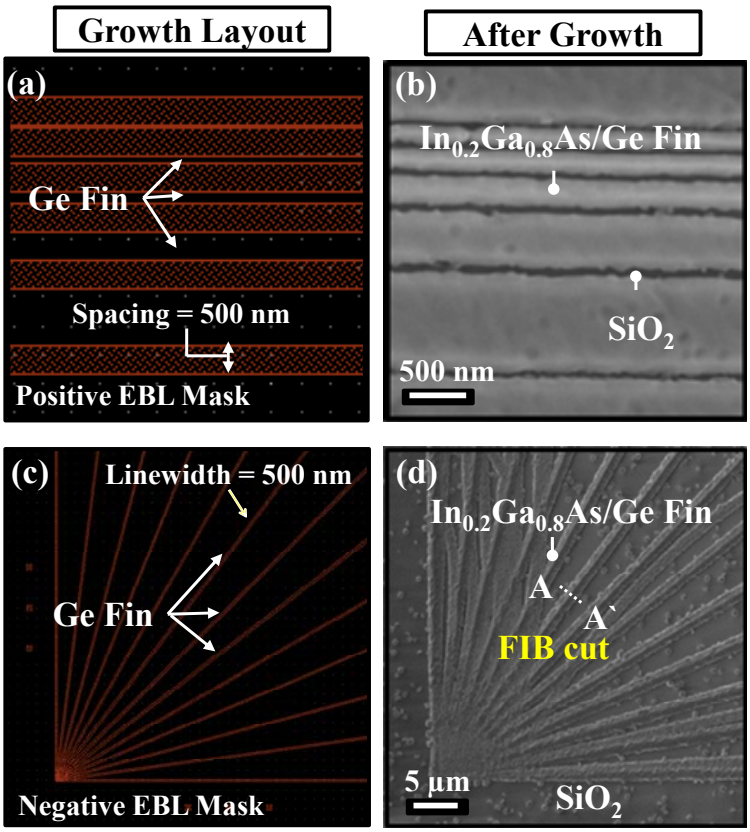


Fig. 3.12 (a) Layout of parallel Ge fins. (b) Top-view SEM image after growth using layout in (a), showing a selective and continuous $In_{0.2}Ga_{0.8}As$ on Ge fins. (c) Layout of Ge fins with different in-plane orientations. (d) Top-view SEM image after $In_{0.2}Ga_{0.8}As$ growth using the layout in (c). The as-grown $In_{0.2}Ga_{0.8}As$ on Ge fins was faceted. FIB cut was performed along the line A-A` for further TEM analysis.

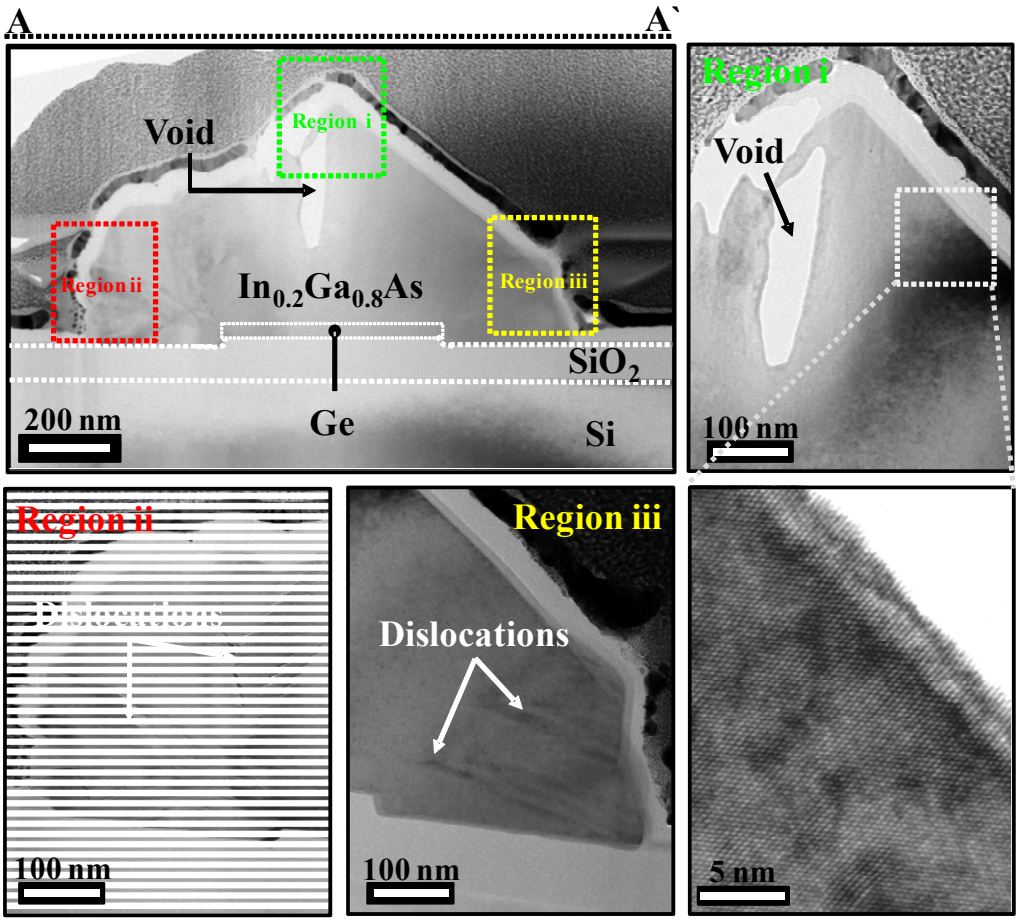


Fig. 3.13 Cross-sectional TEM images (bright-field) of $In_{0.2}Ga_{0.8}As$ fin taken along A-A` from Fig. 3.12. The void was caused by sample preparation. The zoom-in TEM images at the fin's edges (Region ii and Region iii) show high defect densities, while the top side of the fin (Region i) shows good crystalline quality. ZA of the HRTEM image is [010].

Cross-sectional TEM images of the $In_{0.2}Ga_{0.8}As$ fin along A-A` are shown in Fig. 3.13. Zoom-in TEM images on fin edges (Region ii and Region iii) show $In_{0.2}Ga_{0.8}As$ with high defect densities, whereas the top side of the fin (Region i) shows good crystalline quality. The growth mechanism can be understood through the selective and periodic growth of Ge and SiGe on Si within the SiO_2 trench reported in **Error! Reference source not found.**, as shown in Fig. 3.14 (a) and 3.14 (b). Due to lattice mismatch, threading dislocations form at the interface between the epilayer and substrate.

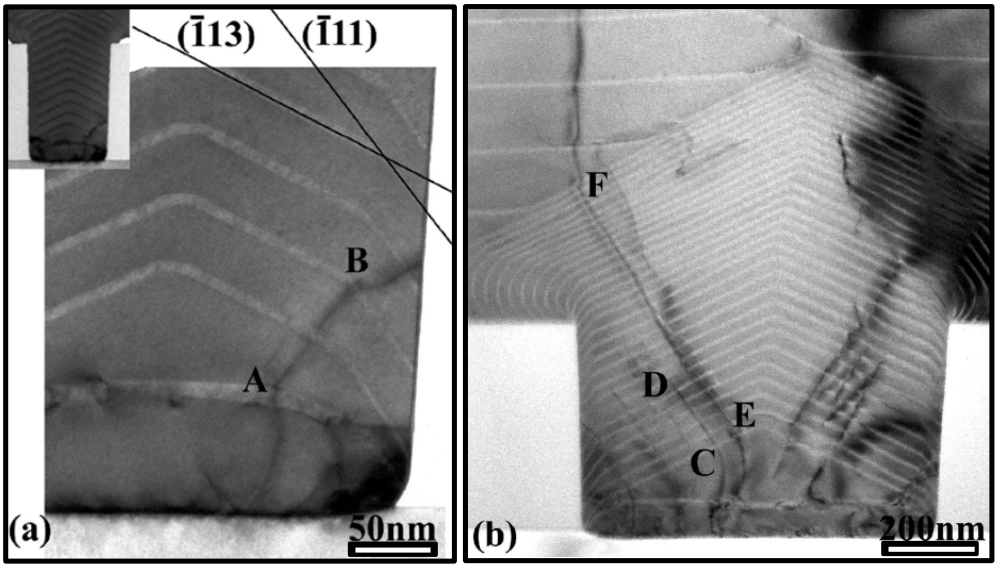


Fig. 3.14 (a) TEM cross section of the Ge/SiGe growth on Si within SiO_2 trench. Periodic growth of Ge and SiGe clearly shows the evolution of the facet with growth time. (b) The propagation of defects was found to be perpendicular to the growth facet. Error! Reference source not found.

The work by Bai et al. Error! Reference source not found. found that the threading dislocations originating at the Ge/Si interface are directed to the trench sidewalls by faceting of the Ge during growth, as shown in Fig. 3.14. The observation is consistent with the preferred directions of growth dislocation lines as proposed by Klapper [120]. In his work, Klapper uses minimum-energy theorem and zero-force theorem to calculate the preferred dislocation directions and found that they are mostly normal or nearly normal to the growth face. Therefore, during the facet formation, the threading dislocations orient themselves perpendicular to the facet during growth, and the angle of the facets directs the dislocations to the sidewall.

3.5 Summary

In this Chapter, a selective growth of GaAs on Ge fins that were formed on 10° offcut GeOI substrate was demonstrated. The dependence of the GaAs facets on fin orientation was modeled and experimentally verified. The GaAs ECS facets were identified based on their inclination angles with respect to the GeOI surface and the growth rate of each facet was extracted. The growth rate ratio for {8 1 1}:{1 1 1}A:{1 1 0}:{1 1 1}B was found to be 18.2:11.2:10:9.2. Furthermore, selective growth of $In_{0.2}Ga_{0.8}As$ on Ge fin were achieved at growth temperature of 640 °C and 95 % filing factor. Our results pave way for possible realization of high mobility III-V/Ge FinFET CMOS on Si platform based on a III-V epitaxy on Ge approach.

Chapter 4

Vertically Stacked III-V Nanowire CMOS on Si Featuring Extremely Thin (Sub-150 nm) Buffer Layer Technology and Common Gate Stack and Contact Modules

4.1 Introduction

III-V semiconductors have been intensely researched as possible alternative channel materials for sub-7 nm technology node logic applications [121]-[131]. To date, one of the main challenges is the cost-effective integration of high mobility and low defectivity III-V channel materials on a Si platform. In Chapter 3, direct growth of GaAs and $In_{0.2}Ga_{0.8}As$ on Ge fin has been demonstrated. However, the nFET device realized by such structures could suffer from sub-surface leakage current due to unfavorable conduction band alignment between $In_xGa_{1-x}As$ with Ge. Furthermore, unintentional doping due to interdiffusion during growth of $In_xGa_{1-x}As$ on Ge could be a potential issue as well. On the other hand, there have been many demonstration of III-V n-channel field-effect-transistors (nFETs) or p-channel field-effect-transistors (pFETs) demonstrated on Si substrate separately using various integration approaches such as growth of thick buffer layer (thicker than 1 μm) [132],[133], double wafer bonding [134],[135], and aspect

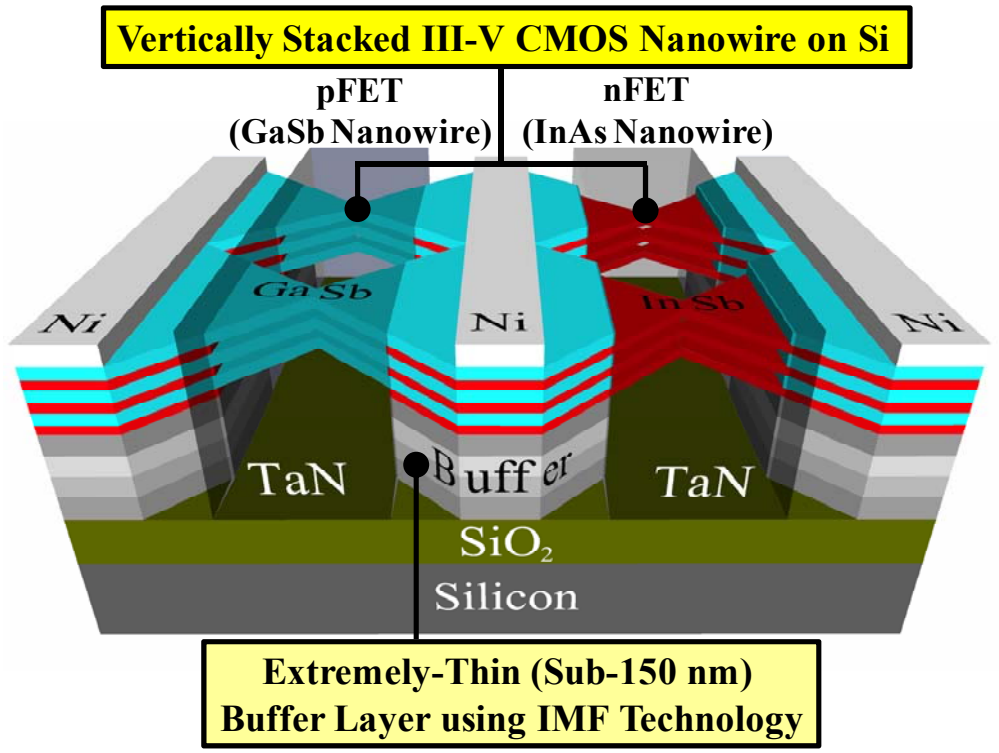


Fig. 4.1 Schematic of vertically-staked III-V CMOS nanowires (NWs) on the Si substrate. Alternating layers of GaSb (pFET channel) and InAs (nFET channel) grown on GeOI allow for the realization of III-V CMOS on a common Si platform. With the introduction of interfacial misfit-defects formation (IMF) technique, the III-V buffer layer stack is as thin as ~150 nm.

ratio trapping (ART) [23]. However, there have been very few reports on III-V complementary-metal-oxide-semiconductor (CMOS) integrated on Si substrate.

The first III-V CMOS on Si substrate featuring InGaSb pFETs co-integrated with InAs nFETs was demonstrated by J. Nah *et al.* using double layer bonding technique [28]. While devices with good performance such as substhreshold swing (*SS*) of 84 mV/decade was achieved for InAs nFET, the integrated devices using double layer bonding technique are not scalable and cannot be applied to sub-7 nm technology node. More recently, researchers from University of Tokyo demonstrated integration of GaSb (or InGaSb) pFETs with InAs nFETs on Si [122], [137]

by layer transfer technique. The active layer comprises of n-channel InAs and p-channel GaSb (or InGaSb) heterostructure. However, both nFETs and pFETs realized by this approach exhibit poor electrical characteristics and suffer from serious ambipolar characteristics. Furthermore, the cost of layer transfer technique is also a major concern.

In addition, to have ultimate control of the short channel effects (SCEs) and to increase on-state current (I_{ON}) at fixed footprint, stacked nanowire (NW) structures are very attractive. Recently, a vertically stacked $In_{0.53}Ga_{0.47}As$ NW was demonstrated by Purdue University [139], showing excellent control of SCEs. However, CMOS realization based on stacked nanowires has not been reported before.

In this Chapter, we demonstrated a novel vertically stacked III-V CMOS NW on Si as shown in Fig. 4.1. In Section 4.2, high-quality InAs and GaSb layers were grown on Ge-on-Insulator (GeOI) through an extremely thin (<150 nm) buffer layer using heteroepitaxy of GaSb on GaAs. This enables the realization of stacked III-V NW CMOS on a common Si platform with sub-500 nm channel length (L_{CH}), as will be discussed in Section 4.3. Subsequently, in Section 4.4, the effect of the NW width (W_{NW}) on *SS* and threshold voltage (V_T) of InAs nFETs was investigated by both experiment and simulation. This is a collaboration work with research team from Nanyang Technological University (NTU) who had contributed the molecular beam epitaxy (MBE) grown epilayer substrate.

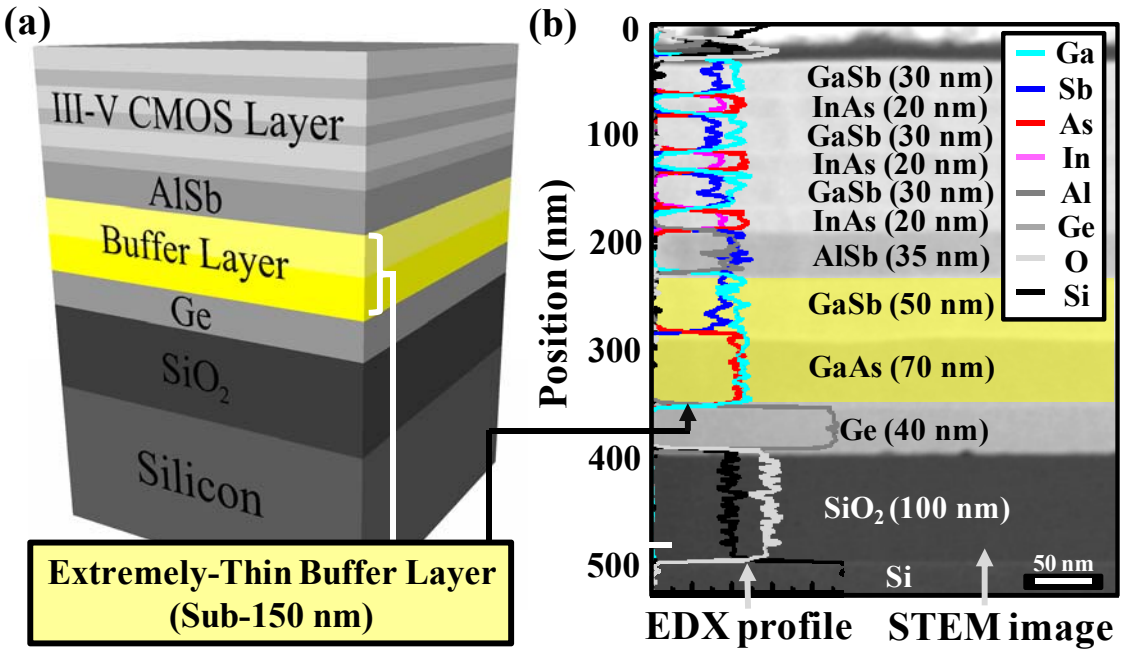


Fig. 4.2 (a) Schematic of the layer structure for realizing III-V CMOS on Si substrate with extremely-thin buffer layer growth technology. (b) Cross-sectional HAADF-STEM image of the III-V layers on Si substrate. Together with EDX profile, three GaSb pFET channel layers and three InAs nFET channel layers are confirmed to be successfully grown. Buffer underneath the InAs/GaSb stack comprise only 50 nm of GaSb and 70 nm of GaAs. This is significantly smaller as compared with other reported in literature (typically larger than 1 μm).

4.2 Extremely Thin Buffer Layer Technology

Fig. 4.2 (a) shows a schematic of the III-V CMOS layer structure on GeOI which is realized using an extremely-thin buffer layer growth technology. The MBE growth processes in this Section were performed by K. H. Tan *et al.* from NTU. The starting substrate is a 6° offcut GeOI (100). The buffer layer comprises of 70 nm of GaAs followed by 50 nm GaSb using molecular beam epitaxy (MBE). A 6° offcut substrate was used to grow the initial GaAs buffer layer on GeOI substrate in order to eliminate the anti-phase domain formation [105]-[106]. It had been suggested that the vicinal surface contains steps of double layer height, providing single-domain template for successive GaAs deposition [136].

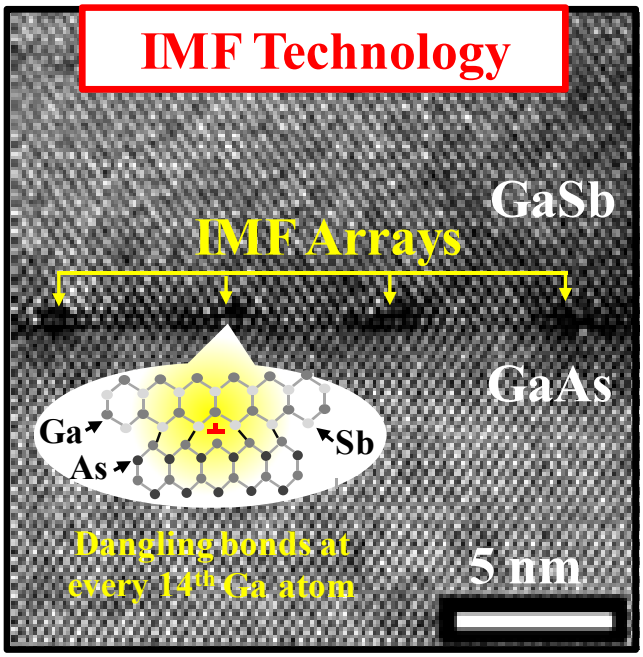


Fig. 4.3 HRTEM image (bright0field) at the GaAs/GaSb buffer layer interface, revealing the growth of high-quality GaSb buffer layer subsequent to the IMF. The HRTEM zone-axis (ZA) is [110]. IMF defects are found to be located within 20 nm of the GaAs/GaSb interface. IMF arrays accommodate the 7.78% compressive lattice mismatch between GaSb/GaAs by forming a dangling bond at every 14th Ga atom. The TEM was performed at Data Storage Institute (DSI) through a service contract.

Another model regards the vicinal surface as a single-layer staircase consists of two types of steps S_A and S_B, according to Chady's notation [137]. It is expected that at the initial stage of growth, only one kind of step is energetically preferable for each atom species, thus providing a perfect atomic stack of polar material atoms [105]-[106]. The 6° offcut surface is necessary to prevent the APD formation in the GaAs layer which could subsequently propagate into the active layers.

The key success of the growth is the interfacial misfit-dislocation formation (IMF) which confines most of the defects within a few nanometers from the GaAs/GaSb interface, enabling subsequent growth of high quality III-V material. The high-angle angular dark field scanning TEM (HAADF-STEM) in Fig. 4.2 (b) depict the various III-V layers grown on GEOI. Energy dispersive X-ray spectroscopy (EDX) line scan overlayed on the HAADF-STEM image [Fig. 4.2 (b)] clearly shows that continuous InAs/GaSb film stack are successfully grown on the thin GaSb/GaAs buffer layers. A regular array of interfacial misfit-defects is formed at the GaAs/GaSb interface as shown by the high-resolution transmission electron microscopy (HRTEM) (bright-field) in Fig. 4.3. The zone-axis of the HRTEM image is [110]. Under specific growth conditions, high quality IMF array can form with a period of ~5.6 nm and can accommodate the 7.78 % lattice mismatch between GaSb and GaAs. It had been reported that the IMF is a 90° edge dislocation defect site which directs the propagation of the defects perpendicular to the growth plane, resulting in a high-quality growth of the active layer [140]. The HRTEM image in Fig. 4.3 also shows that high-quality GaSb buffer was achieved within sub-20 nm growth subsequent to the IMF formation, suggesting that further reduction of the buffer layer thickness is possible.

The InAs/GaSb multilayer heterostructure was investigated by cross-sectional TEM (bright-field) measurement and analysis as shown in Fig. 4.4 (a). Since the lattice mismatch between InAs and GaSb is about 0.62 %, InAs/GaSb interface is tensile (T) and GaSb/InAs interface is compressive (C). In order to balance the strain, equal number of C/T layers was grown. From Fig. 4.4 (a), it can be seen that the epilayers were homogeneous and have a smooth heterointerface. A zoom in view high-resolution TEM image (bright-field) in Fig. 4.4 (b) shows a sharp interface, where the lattice line can be seen to extend across the GaSb and InAs layer.

Atomic force microscope (AFM) scan with a 3 μm × 3 μm scan area reveals a root mean square (r.m.s) value of 2.51 nm, as shown in Fig. 4.4 (c). On this sample, pit-holes can be seen from the AFM image, likely due to threading dislocation that propagates from the GaAs/GaSb interface. The pit-holes and the surface roughness can be further improved by calibrating the growth conditions. In a recemt follow up work done by Tan et al. [141], r.m.s value a small as 0.5 nm was achieved by optimizing the growth temperature. This value is comparable to the best reported r.m.s value for thick buffer layer.

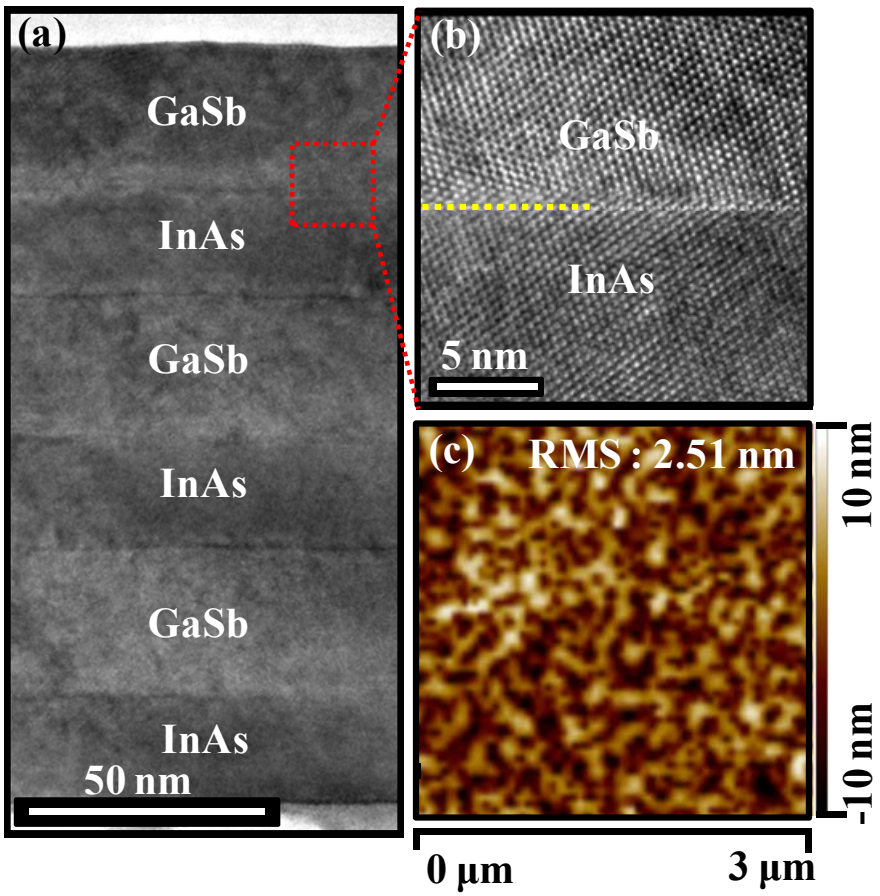


Fig. 4.4 (a) TEM image (bright field) of the active layers comprising of InAs/GaSb stacked layers. (b) Zoom in view HRTEM image (bright-field) at the InAs/GaSb interface, showing the high-quality of InAs and GaSb layers. (c) AFM surface scan of the grown layer structure reveals RMS value of 2.51 nm. The zone axis (ZA) of the TEM images are [110]. The TEM was performed at DSI through a service contract.

Table 4.1 Advantages of thin buffer layer technology as compared to other state-of-art III-V on Si integration techniques.

Integration Technique	Low Cost	Simple Process	High Film Quality	Scalable to 12" and above
Layer Transfer	×	×	√	×
Nanohetero epitaxy	√	√	×	√
ART	√	√	×	√
Thick Buffer	×	√	√	√
Thin Buffer	√	√	√	√

Table 4.1 shows the advantages of thin buffer layer growth technique as compared to other state-of-art integration techniques, including aspect-ratio-trapping, nanoheteroepitaxy, layer transfer, and thick buffer layer. In terms of cost, thin buffer layer compares favorably with thick buffer layer technology since more than 10 times reduction in buffer layer thickness can be achieved. Furthermore, the integration process is simple and does not require nano-trench patterning used in ART and nano-structure formations used in nanoheteroepitaxy. In addition, thin buffer layer technology has high scalability, which is the ability of an integration approach to be applied on the Si substrate with growing wafer size. Thin buffer layer technology can be used to integrate III-V materials on 12" or larger Si substrate.

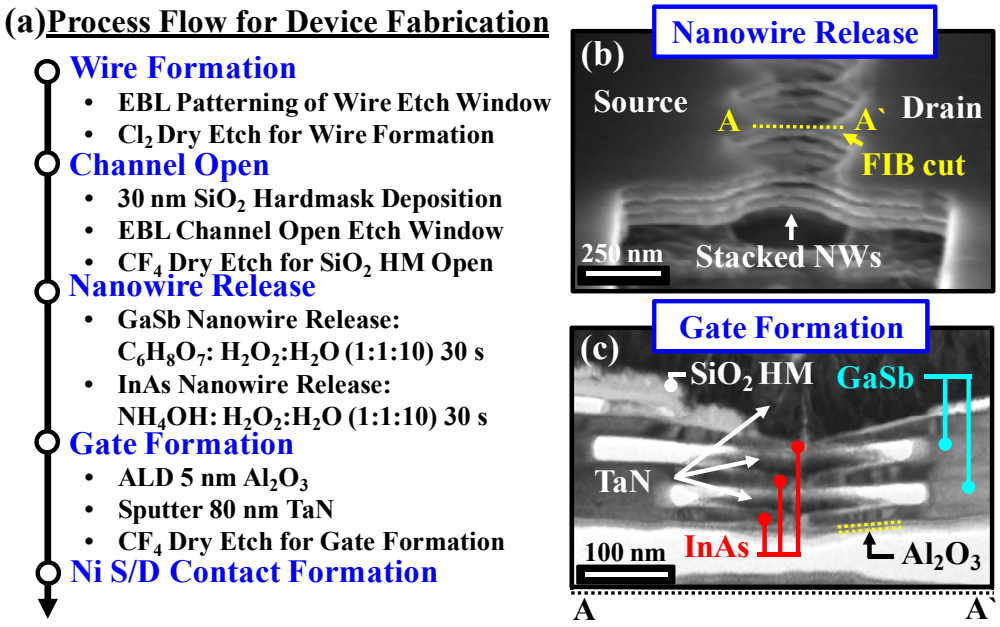


Fig. 4.5 (a) Process flow for fabrication of vertically stacked III-V NW CMOS. (b) Tilt-view SEM showing the successful formation of vertically stacked NWs after the NW release step. (c) Cross-sectional TEM image (bright-field) of the stacked InAs NW FETs cutting along line A-A' in (b). The InAs wires have height of ~20 nm and are surrounded by the Al_2O_3 high-*k* gate dielectric.

4.3 Realization of Vertically Stacked III-V NW CMOS

Key process flow for the realization of vertically stacked III-V NW CMOS is shown in Fig. 4.5 (a). First, diamond-shaped etch windows with spacing ranging from 80 to 160 nm and in steps of 2 nm were defined by electron beam lithography (EBL). This was followed by photoresist trimming using O_2 plasma at 180 °C for 10 s. The trimming rate was calibrated such that NW with W_{NW} down to 6 nm can be achieved. This is followed by anisotropic dry etching of the InAs and GaSb layers using chlorine (Cl_2) and hydrogen (H_2)-based plasma at 250 °C to achieve NWs with vertical sidewalls.

30 nm-thick SiO_2 was then deposited as the hard-mask for the subsequent channel open step and followed by CF_4 plasma etching. The channel open step defines the L_{CH} of the

device and serves as a wet etch mask to prevent excess undercut of the AlSb layer during the NW release step. This is crucial as the etchant used for the InAs and GaSb NWs release in the subsequent step can also etch AlSb buffer layer rapidly with etch rate of ~ 50 nm/s, causing InAs or GaSb NWs to collapse onto the substrate.

After that, InAs NWs were released using $NH_4OH:H_2O_2:H_2O$ (1:1:10) solution to etch the GaSb layers, and GaSb NWs were released using $C_6H_8O_7:H_2O_2:H_2O$ (1:1:10) to etch the InAs layers. The $C_6H_8O_7:H_2O_2:H_2O$ solution was calibrated to etch InAs at ~ 1 nm/s with InAs over GaSb selectivity of 80:1. Meanwhile, $NH_4OH:H_2O_2:H_2O$ solution was calibrated to etch GaSb at ~ 0.2 nm/s with GaSb over InAs selectivity of 10:1.

Tilt-view scanning electron microscopy (SEM) image of the vertically stacked InAs NWs is shown in Fig. 4.5 (b). The stacked nanowires are well formed. There is an evident undercut underneath the InAs stacked nanowires. This is because the buffer layers which comprise of AlSb, GaSb, GaAs, and Ge can be etched by the $NH_4OH:H_2O_2:H_2O$ (1:1:10) solution during the GaSb release steps. Similar undercut profile was also observed for the GaSb stacked nanowires.

This is followed by the deposition of 5 nm-thick Al_2O_3 using atomic layer deposition (ALD) and 80 nm-thick TaN metal gate using sputter. Prior to the Al_2O_3 gate deposition, the InAs and GaSb surfaces were treated in sulfur solution to passivate the surface dangling bonds. Finally, 80 nm-thick Ni layer was deposited in the S/D regions to form the Ohmic contact. Fig. 4.5 (c) shows the cross-sectional transmission electron microscope (TEM) image of a completed InAs transistor cutting along the dashed line A-A'. The InAs NWs are successfully released and have height of 20 nm and are surrounded by the Al_2O_3 and TaN metal gate.

4.4 Device Characterization

4.4.1 Electrical Characterization

Fig. 4.6 shows the drain current versus gate voltage (I_D-V_G) curves of a GaSb NW pFET with L_{CH} of 500 nm. The I_D values are normalized by the device effective width (W_{eff}) which is the sum of the total nanowire width ($2\times n\times W_{NW}$) and nanowire height ($2\times n\times H_{NW}$) where n is the number of nanowires. Good transfer characteristics with on-state/off-state drain current ratio (I_{ON}/I_{OFF}) of over 10^3 were observed. This device exhibit record low substhreshold swing (*SS*) of 188 mV/decade for all GaSb pFETs on Si reported to date. Drain induced barrier lowering (*DIBL*) of 140 mV/V was achieved at drain current (V_D) of 0.5 V. I_D-V_D curves of the device in Fig. 4.7 show good pinch-off and saturation characteristics. However, it should be noted common high-k metal gate stack (HKMG) module involving TaN/Al_2O_3 which was adopted in our experiment was not optimized for GaSb pFET. It has been reported that the interface of Al_2O_3 and GaSb which are not optimized can suffer from high D_{it} of more than 2.5×10^{12} cm^{-2} [8]. This lead to substhreshold-swing (*SS*) degradation despite having large gate length and small V_D=-0.05 V.

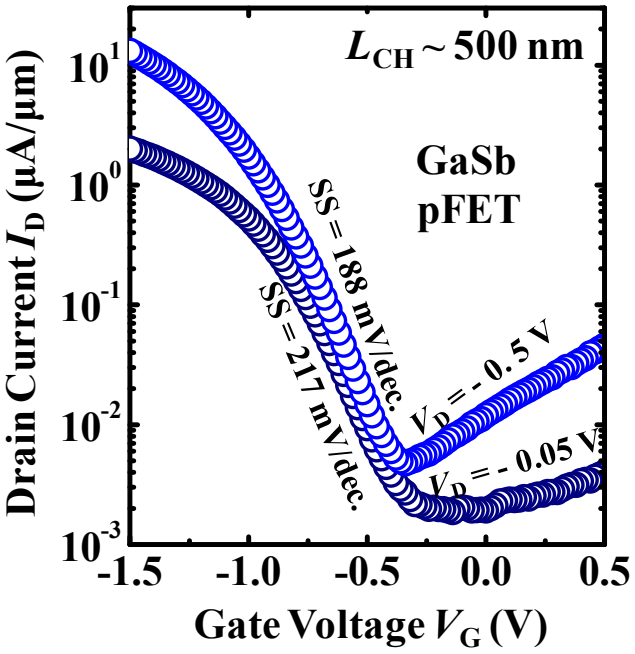


Fig. 4.6 I_D-V_G of the GaSb NW pFET with 500 nm L_{CH}, showing excellent I_{ON}/I_{OFF} ratio more than 3 orders of magnitude, *SS* of 188 mV/decade, and *DIBL* of 140 mV/V.

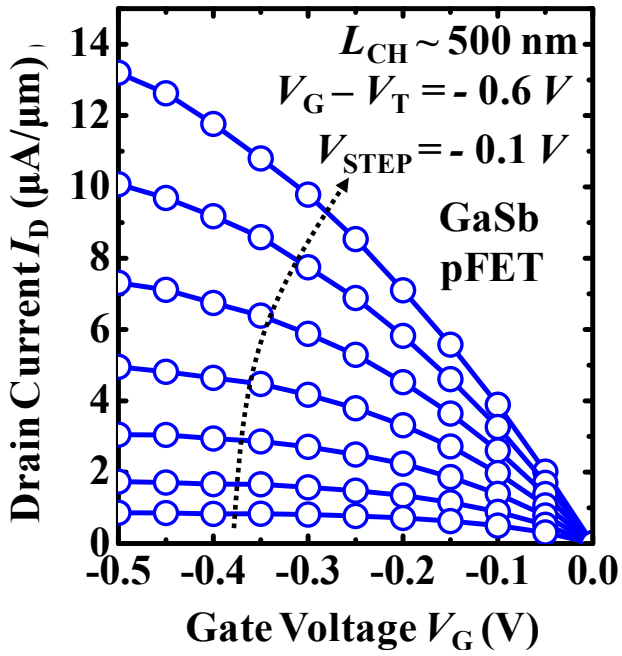


Fig. 4.7 I_D-V_D of the same device in Fig. 4.7 showing good pinch-off and saturation characteristics.

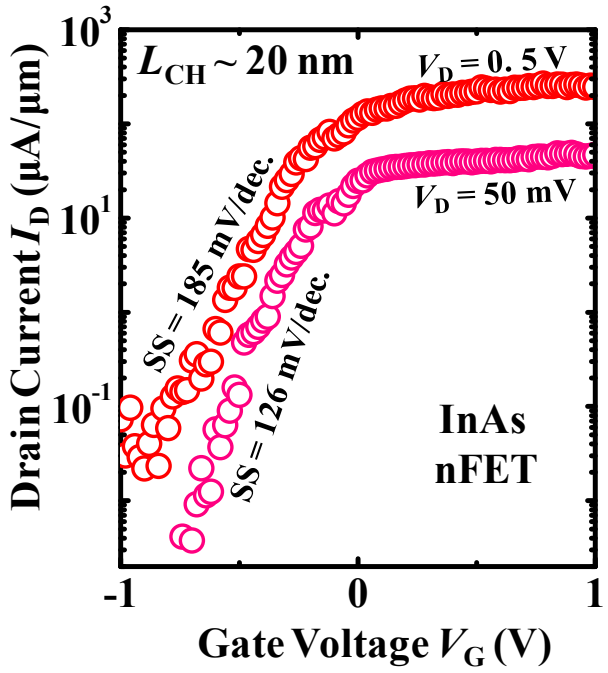


Fig. 4.8 I_D-V_G of the InAs NW nFET with L_{CH} of 20 nm. Excellent transfer characteristics were achieved with I_{ON}/I_{OFF} ratio of ~4 orders, *SS* of 126 mV/decade, and *DIBL* of 285 mV/V.

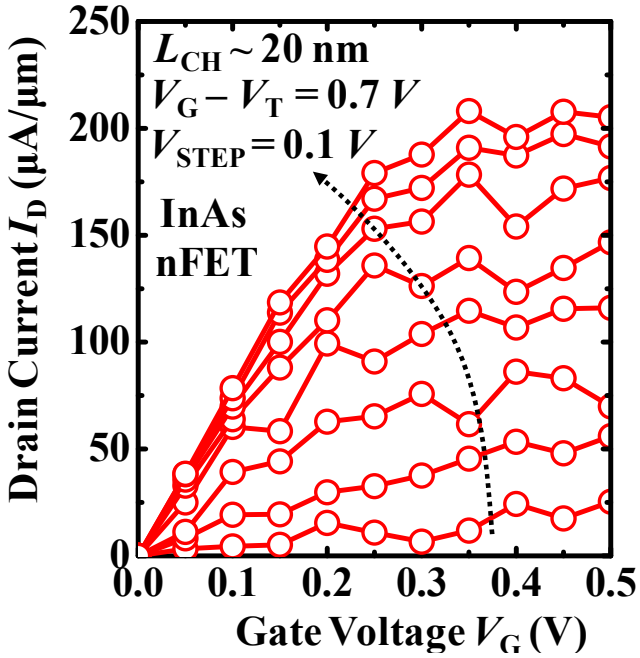


Fig. 4.9 I_D-V_D of the same device in Fig. 4.9 showing good pinch-off and saturation characteristics. I_{ON} of 175 μA/μm was achieved at V_D of 0.5 V and V_G-V_T of 0.5 V.

The gate overdrive (V_G-V_T) where V_T is the threshold voltage obtained by linear extrapolation at V_D of 0.05 V was varied from 0 to -0.6 V with steps of -0.1 V. Better *SS* and *DIBL* could be achieved by reducing the effective oxide thickness (EOT) and by further optimization to reduce the nanowire surface damage.

I_D-V_G curves of the InAs NW n-FET with a L_{CH} of 20 nm are shown in Fig 4.8. Good transfer characteristics were observed with *SS* of 126 mV/decade, *DIBL* of 285 mV/V, and I_{ON}/I_{OFF} ratio of over 10^4. The I_D-V_D characteristics in Fig. 4.9 show good pinch-off and saturation characteristics. V_G-V_T was varied from 0 to 0.7 V with steps of 0.1 V. High I_{ON} of 175 μA/μm was achieved at V_D and V_G-V_T of 0.5 V. The drive current performance could be further enhanced by adopting self-aligned S/D metal contact schemes and scaling down the EOT [45]-[50]. The noise in the InAs nFETs could arise from the non-uniformity in the nanowires width due to the surface roughness generated by plasma etching processes. This lead to threshold voltage variability among the different nanowires, and thus causing the noise in the drain current of InAs nFET.

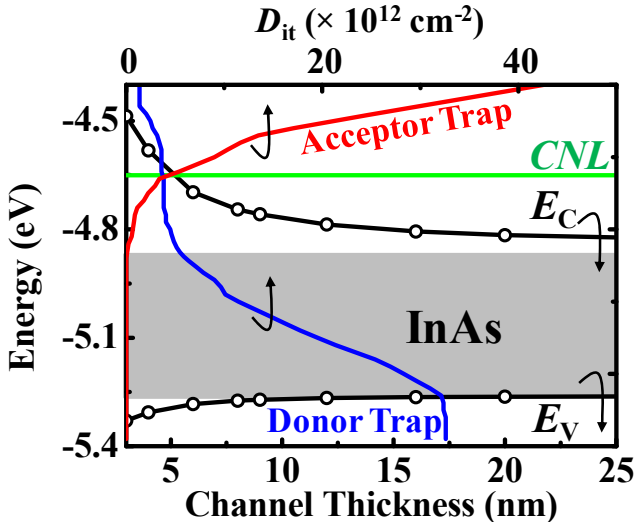


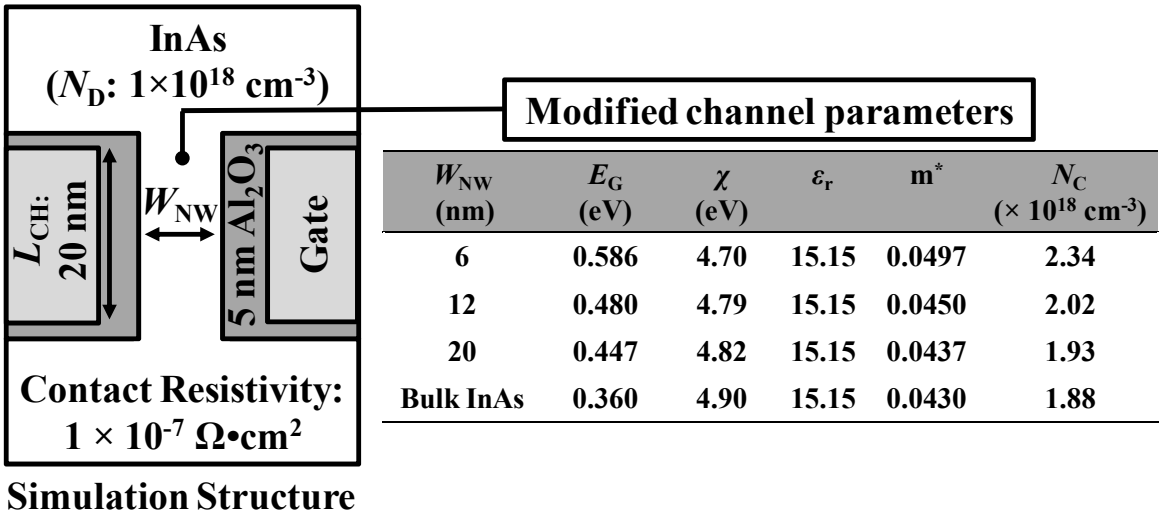
Fig. 4.10 Bandgap of InAs as a function of channel thickness. The D_{it} profile was obtained from [146]. The charge neutrality level (CNL) is assumed to be independent of channel thickness in our simulation. As W_{NW} decreases, the bandgap of InAs widens. This changes the relative position of InAs conduction band edge with the *CNL*, and therefore affects the electrical characteristics of InAs nFETs.

4.4.2 Effect of InAs W_{NW} on the Electrical Characteristics of InAs nFETs

To investigate the effect of W_{NW} on the electrical characteristics of InAs nFETs, a model is proposed in Fig. 4.10 (a). The position of *CNL* is determined by the weights of conduction-band (acceptor-like states) and valence-band derived states (donor-like states) [147]. If the Fermi level lies below *CNL*, ionized empty donor-like states build up a large positive interface charge. On the other hand, if the Fermi level is above the *CNL*, occupied acceptor states lead to negative interface charges. Energy considerations thus make it favorable for the Fermi level to be located at the *CNL*. InAs nFETs with Al_2O_3 gate stack have been shown to suffer from high density of interface states (D_{it}), leading to strong Fermi level pinning at ~0.15 eV above the InAs conduction band edge [146]. Reducing W_{NW} increases the band-gap of InAs, especially when W_{NW} is less than 10 nm. This changes the relative position between the conduction band edge of InAs and the *CNL*, thus affecting the electrical characteristics of InAs nFETs. In Fig. 4.10, InAs

bandstructures are simulated using the $sp^3d^5s^*$ tight-binding (TB) model with the consideration of the effect of spin-orbit coupling. The thickness of InAs is varied from 6 nm to 20 nm. The sp3d5s* tight-binding parameters for InAs was obtained from [142]. Surface dangling bond were passivated with hydrogen to remove the gap states in the TB.

The proposed mechanism is further investigated using a 2D device simulation structure illustrated in Fig. 4.11 where the modified bandgap, electron affinity, and intrinsic charge concentration obtained from tight-binding calculation are used as the material properties of InAs channel for transport simulation. Donor doping concentration of 1×10^{18} cm^{-2} is specified for InAs. For the gate stack, 5 nm Al_2O_3 and metal gate with work function of 4.9 eV are defined in our simulation. Contact resistivity value of 1×10^{-7} $\Omega\cdot cm^2$ was defined at in the S/D contact region. In addition, D_{it} profile obtained from [146] is specified at the InAs/Al_2O_3 interface.



W_{NW} (nm)	E_G (eV)	χ (eV)	ε_r	m*	N_C (× 10^{18} cm^{-3})
6	0.586	4.70	15.15	0.0497	2.34
12	0.480	4.79	15.15	0.0450	2.02
20	0.447	4.82	15.15	0.0437	1.93
Bulk InAs	0.360	4.90	15.15	0.0430	1.88

Fig. 4.11 Device structure and key parameters defined for the simulation. The InAs parameters were obtained from $sp^3d^5s^*$ tight-binding (TB) model with the consideration of the effect of spin-orbit coupling.

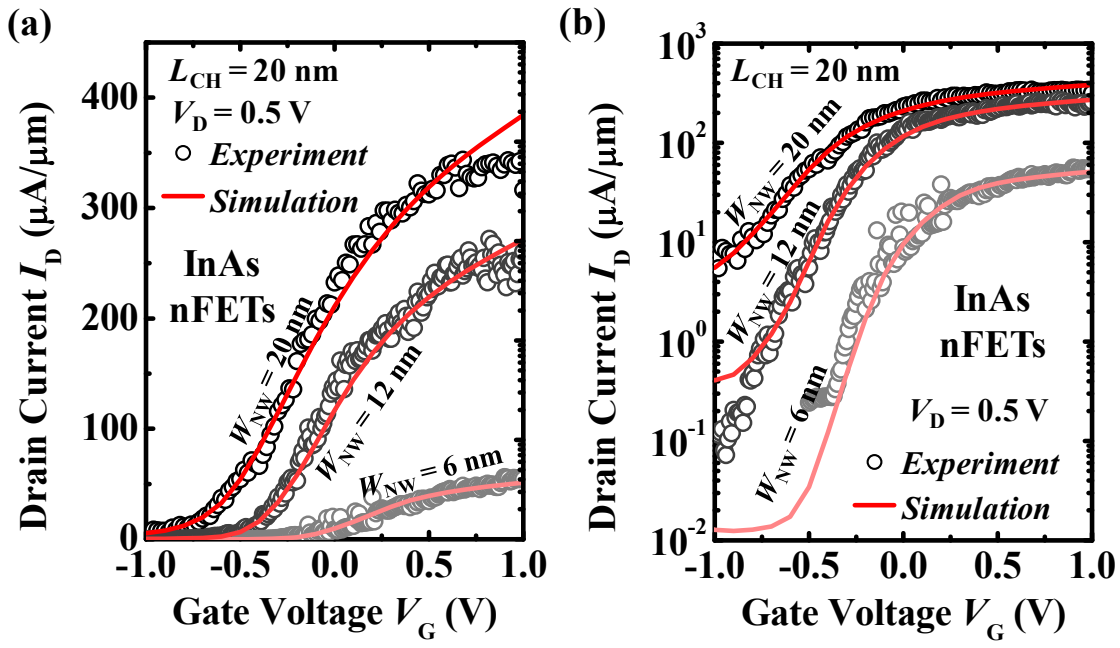


Fig. 4.12 Simulated and experimental (a) linear I_D-V_G plot and (b) logarithmic I_D-V_G plot for InAs NW nFETs with L_{CH} of 20 nm and V_D of 0.5 V for W_{NW} of 6 nm, 12 nm, and 20 nm. Smaller *SS* and positive shift of V_T were observed with decreasing W_{NW}. Using band structure parameters and interface trap distribution shown in Fig. 4.13, the simulated I_D-V_G curves of InAs nFETs show an excellent agreement with the experimental results.

Fig. 4.12 compares the experimental and simulated I_D-V_G curves for InAs NW nFETs with a fixed L_{CH} of 20 nm but different W_{NW} of 20 nm, 12 nm, and 6 nm. V_D is fixed at 0.5 V. Using the simulation parameters defined in Fig. 4.11, the simulated I_D-V_G curves show good agreement with the experimental results. The discrepancy in the on-state current level between simulation and experimental result for device with W_{NW} of 20 nm could be due to the variation in the specific contact resistivity from device to device. Plots of *SS* and V_T as a function of W_{NW} for InAs nFETs with L_{CH} of 20 nm are shown in Fig. 4.13 (a) and Fig. 4.13 (b), respectively. Both the experimental *SS* and V_T values were extracted at V_D of 0.5 V.

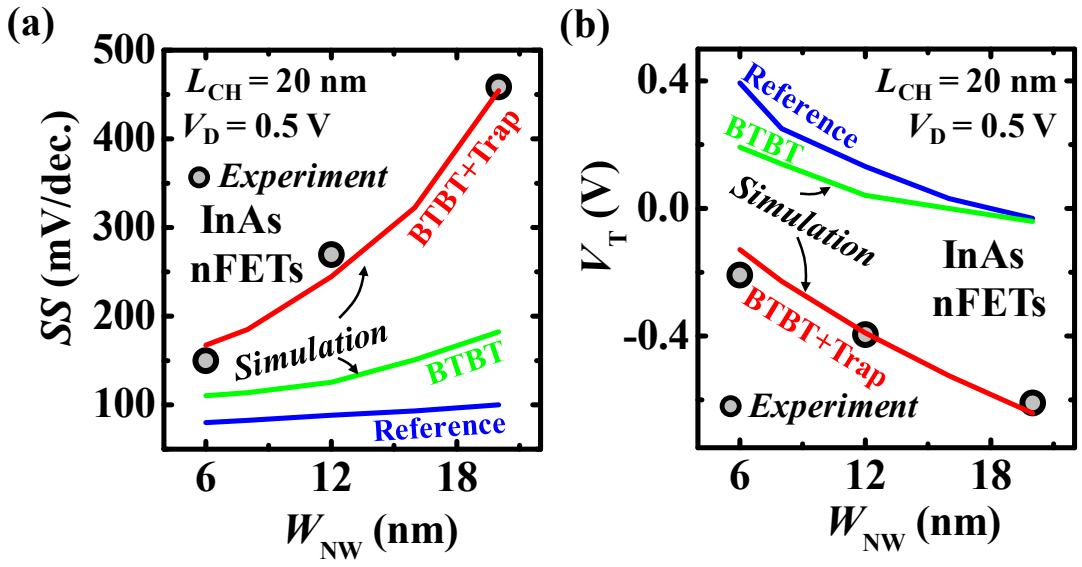


Fig. 4.13 Plot of (a) *SS*-W_{NW} and (b) V_T-W_{NW} for InAs NW nFETs with L_{CH} of 20 nm and V_D of 0.5 V. Obvious decrease in *SS* and positive shift in V_T were observed with reducing W_{NW}. In both figures, the open symbols are experimental data for InAs devices with W_{NW} of 6 nm, 12 nm and 20 nm. Meanwhile, the color lines are simulation results for devices with BTBT and trap modeling (red lines), BTBT only (green lines), and reference devices without consideration of BTBT and interface traps (blue lines). By considering interface traps in our simulation, excellent agreement between the simulated and experimental results can be obtained.

Significant reduction of *SS* and obvious positive shift of V_T were observed with decrease in W_{NW}. The blue lines in Fig. 4.13 are simulation results without considering the effect of BTBT and interface traps. It can be clearly seen that without the consideration of BTBT and interface traps, the simulation results severely underestimate the *SS* degradation and V_T shifts in our InAs devices. Furthermore, it is also obvious that BTBT mechanism (green line in Fig. 4.13) alone was unable to account for the huge change of the *SS* and V_T. On the other hand, by including the proposed trap model along with BTBT mechanism, our simulation results (red line in Fig. 4.13) were able to fit the experiment data well. Our results suggest that interface traps play a significant role in the electrical characteristics of InAs nFETs.

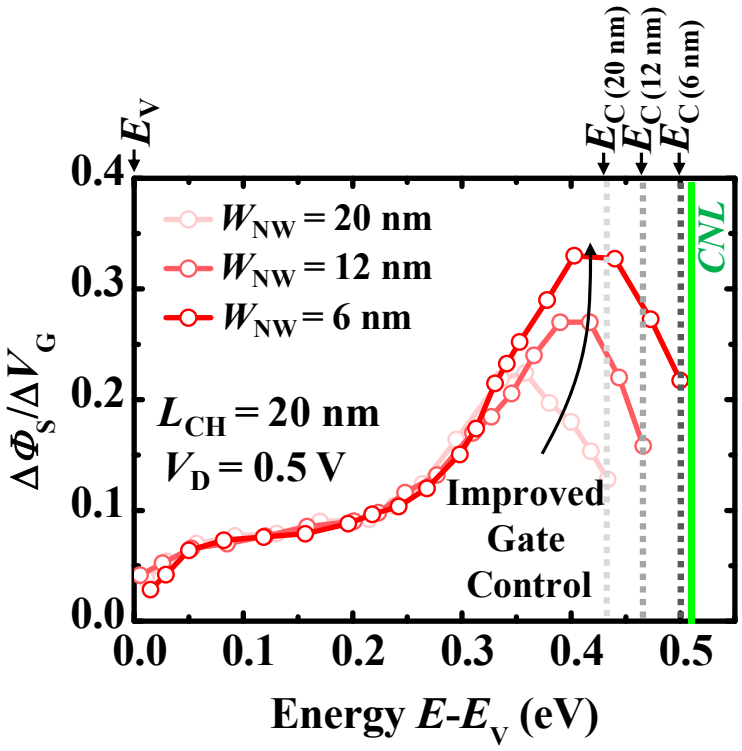


Fig. 4.14 The change of surface potential relative to the gate voltage ($\Delta\Phi_s/\Delta V_G$) at different quasi Fermi level (E_{QFL}) within InAs bandgap for W_{NW} of 6 nm, 12 nm, and 20 nm. As W_{NW} decreases, InAs conduction band-edge shift closer to *CNL*, resulting in lower density of donor-like traps near the conduction band. This enhanced the $\Delta\Phi_s/\Delta V_G$ for E_{QFL} near the InAs conduction band due to easier detrapping of the traps.

Fig. 4.14 shows the change of surface potential relative to the gate voltage ($\Delta\Phi_s/\Delta V_G$) at different quasi Fermi level (E_{QFL}) within InAs bandgap for W_{NW} of 6 nm, 12 nm, and 20 nm. The energy reference level was taken at the valence band of InAs (E_V = 0 eV). As W_{NW} decreases, InAs conduction band-edge shift closer to *CNL*, resulting in lower density of donor-like traps near the conduction band. This enhances the $\Delta\Phi_s/\Delta V_G$ for E_{QFL} near the InAs conduction band due to easier detrapping of the donor-like traps. As the results, the *SS* of the InAs nFET improves.

However, as W_{NW} decreases, the acceptor traps density above the conduction band of InAs also increases at the same time. The presence of high density acceptor traps have been reported to degrade the device mobility [148],[149]. The acceptor-like traps are neutral when empty and negatively charged when ionized. Filling acceptor-type traps results in net negative charges buildup at the interface, which causes Coulomb scattering and degrades nFETs mobility. All these observations are consistent with our experimental results.

4.4.3 Benchmarking

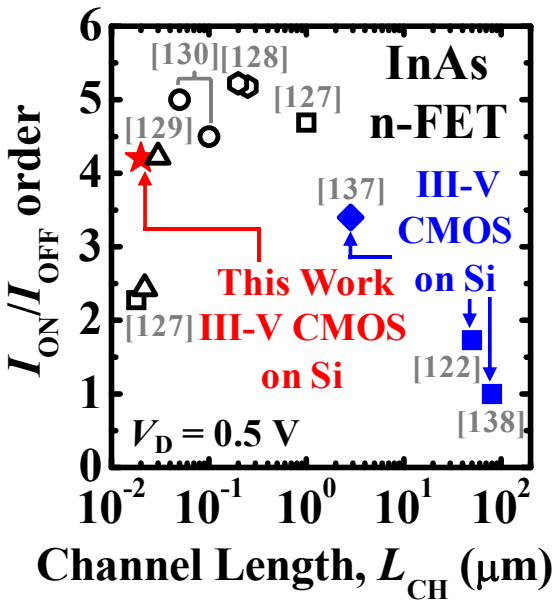


Fig. 4.15 Benchmark plot comparing I_{ON}/I_{OFF} ratio of InAs nFET in this work with other InAs nFETs reported in literature. High I_{ON}/I_{OFF} of 4 orders was achieved for InAs nFET realized in this work at V_D of 0.5 V and L_{CH} of 20 nm. This is the best value for III-V CMOS on Si substrate.

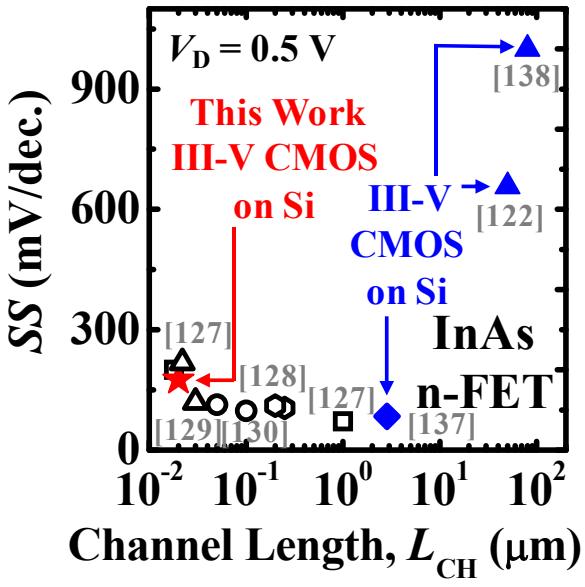


Fig. 4.16 Benchmark plot comparing *SS* of InAs nFET in this work with other InAs nFETs reported in literature. Low *SS* of 185 mV/decade was achieved for InAs nFET realized in this work at V_D of 0.5 V and L_{CH} of 20 nm.

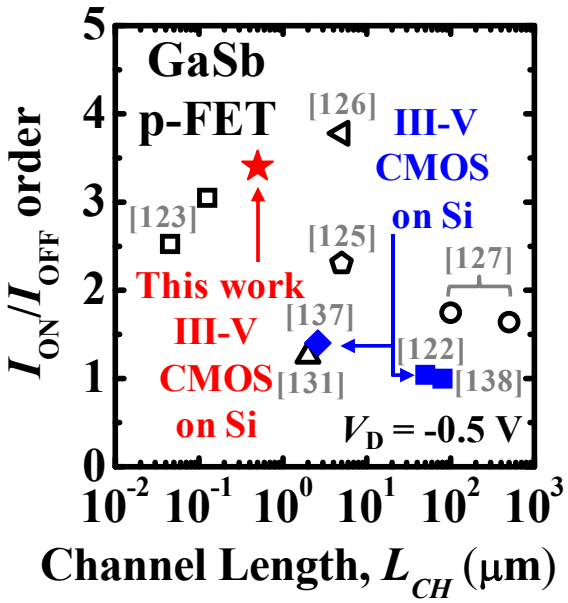


Fig. 4.17 Benchmark plot comparing I_{ON}/I_{OFF} ratio in this work with other GaSb pFETs reported in literature. High I_{ON}/I_{OFF} of 3.5 orders was achieved for GaSb pFET realized in this work at V_D of 0.5 V. This is the best value for III-V CMOS on Si substrate.

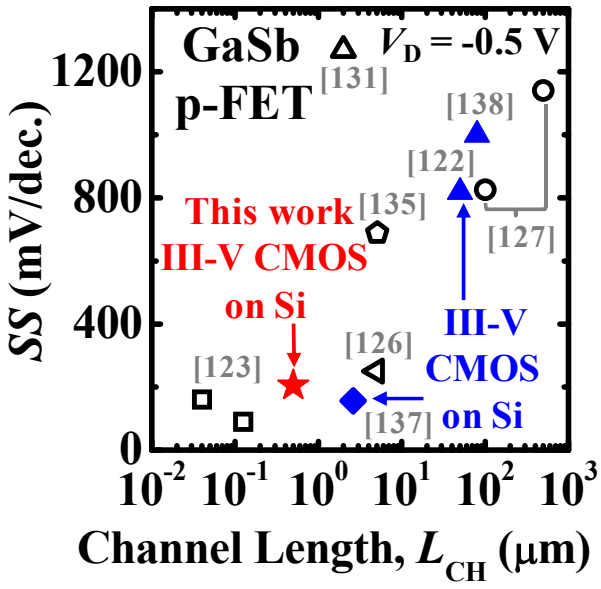


Fig. 4.18 Benchmark plot comparing *SS* of GaSb pFET in this work with other GaSb pFETs reported in literature. The GaSb FETs realized in this work achieved the low *SS* of 188 mV/decade. This is the best value for GaSb pFETs on Si.

Fig. 4.15 to Fig. 4.18 benchmark *SS* and I_{ON}/I_{OFF} ratio of InAs nFET and GaSb pFET in this work with other reported values in literature. The filled symbols are CMOS devices realized on Si, similar with our work. Meanwhile, the open symbols are individual devices realized either on Si or III-V substrates. For InAs nFETs, the devices realized in this work achieved low *SS* of 126 mV/decade and highest I_{ON}/I_{OFF} of 10^4 for III-V CMOS on Si substrate. For GaSb pFETs, the I_{ON}/I_{OFF} (more than 10^3) and *SS* (188 mV/decade) compete well with the best reported on III-V substrate and are much better than those of III-V CMOS on Si substrate.

4.5 Summary

In this Chapter, the first demonstration of vertically stacked III-V nanowire (NW) CMOS was presented. The InAs nFETs and GaSb pFETs were integrated on a common Si platform using a cost-effective extremely-thin (sub-150 nm) buffer layer technology for the first time. Decent transfer characteristics with *SS* of 126 mV/decade and *DIBL* of 285 mV/V were achieved for the InAs nFET with L_{CH} of 20 nm. For the vertically stacked GaSb NW pFET with a L_{CH} of 500 nm, lowest reported *SS* of 188 mV/decade and highest I_{ON}/I_{OFF} ratio of more than 10^3 were achieved for GaSb pFETs on the Si substrate. Furthermore, the effect of InAs nanowire thickness on the electrical characteristics of InAs nanowire FETs was also investigated by simulation and experiment. The results from this Chapter could pave the way for realization of cost-effective III-V CMOS on a common Si substrate for future high-performance and low-power logic application.

Chapter 5

Short Channel Nanowire with Tapered S/D Structure and Quantum Dots with Self-Aligned S/D Structure

5.1 Introduction

As the scaling of complementary-metal-oxide-semiconductor (CMOS) rapidly approaches the end-of-roadmap, the search for ultimate device architectures and new device technologies beyond CMOS has increased in the past decade [150]-[154]. III-V nanowire field-effect transistor (NWFETs) with a thin nanowire channel is considered as one of the promising candidates for sustaining the scaling of CMOS to the end-of-roadmap since their non-planar geometry provide superior gate electrostatic control as compared to the conventional planar structures [155]-[163]. In Chapter 4, we have demonstrated that a device architecture comprising stacked NWs exhibits good control of short channel effects (SCEs). However, the nanowire architecture suffers from high series resistance in the nanowire source/drain (S/D) extension region (L_{EXT}), which would compromise drive current (I_D) performance.

Single electron transistors (SETs) have also been considered as another possible candidate for future low power and high density integrated circuits because of their potential for ultra-low power operation involving only a few electrons [164]-[166]. However, in order for SETs to be useful in practical applications, it must be operated at room temperature. Recently, several experimental demonstrations of SETs that can operate at room temperature have been reported [167]-**Error! Reference source not found.**. This includes the work done by K.

Matsumoto *et al.* **Error! Reference source not found.** where their SETs have typical quantum dot island size of 30-50 nm by 30-50 nm. However, the SETs were fabricated using scanning tunneling microscope (STM) which are not suitable for large scale production.

In this Chapter, we present two novel device architectures as potential candidates for end-of-roadmap and beyond CMOS scaling. These devices were realized by exploiting the anisotropic wet etch profile of III-V materials. In Section 5.2, an in-depth analysis on anisotropic wet etch profile of III-V material was performed. A physical model for wet etching was proposed and verified through extensive experimental results. In Section 5.3, we exploit the anisotropic wet etch profile of III-V materials to realize a novel NW with tapered S/D structure. NWFETs with channel length (L_{CH}) down to 14 nm were. Finally, in Section 5.4, a novel quantum dot with self-aligned S/D structure was realized. Using a self-limiting anisotropic wet etch process, regular shaped-quantum dots with size down to 30-40 nm by 40-60 nm were achieved.

5.2 Modeling of Indium Arsenide (InAs) Anisotropic Wet Etch

5.2.1 Wet Etching Mechanism of InAs

Wet etching is a process that removes material from a substrate surface by chemical solution(s). The mechanism of wet etching of III-V compound semiconductor normally requires three important agents, which are oxidizing agent, acid (or alkali), and water. The oxidizing agent oxidizes the atoms (oxidation) on the semiconductor surface, followed by the dissolution of the oxidized atoms (reduction) in acid (or alkali) [170]. In our wet etch experiment, we focused primarily on InAs substrate, but it is applicable to a wide variety of III-V semiconductors as well. Considering oxidation reaction (M = In or As)

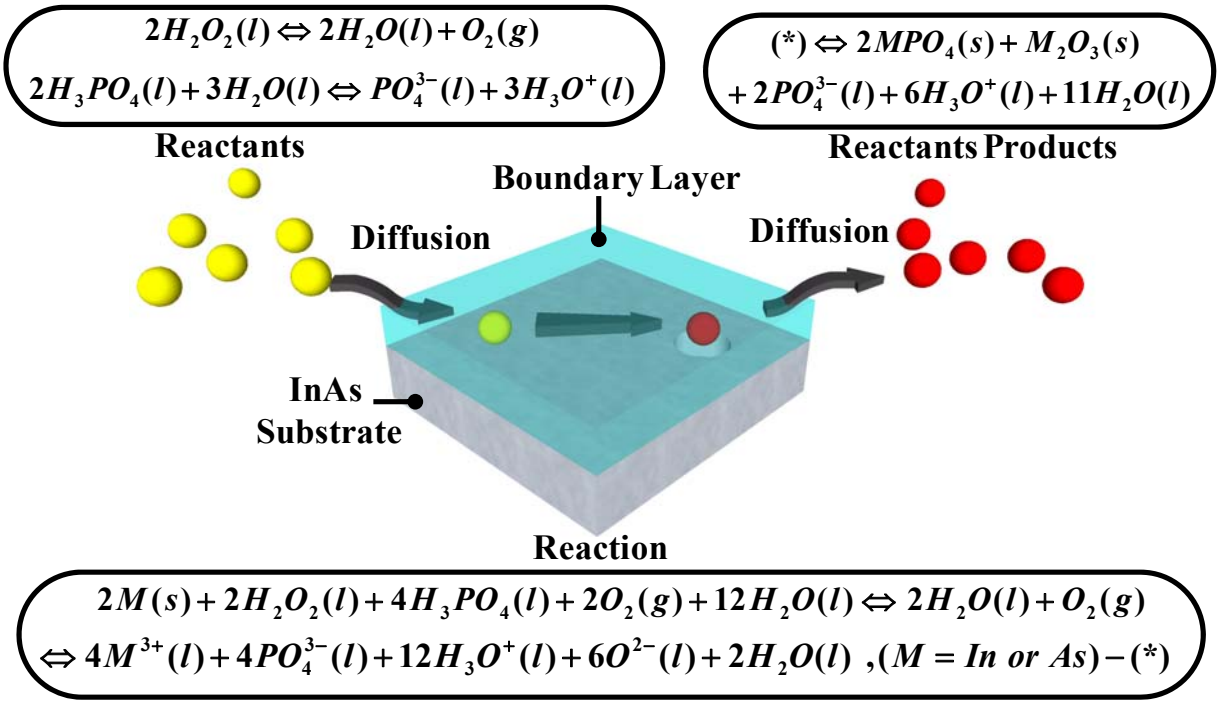


Fig. 5.1 Schematic showing wet etch process of InAs by H_3PO_4:H_2O_2:H_2O (1:1:20). Key processes that occur during wet etch are diffusion of reactants through boundary layer, adsorption of reactants on surface, surface reaction, and diffusion of by-products formed during reaction.

$$M(s) \Leftrightarrow M^{3+}(l) + 3e^-, \text{ (oxidation reaction)} \tag{5.1}$$

and reduction reaction

$$O_2(g) + 4e^- \Leftrightarrow 2O^{2-}(l), \text{ (reduction reaction)} \tag{5.2}$$

the result of oxidation/reduction is

$$4M^{3+}(l) + 6O^{2-}(l) \Leftrightarrow 2M_2O_3(s). \tag{5.3}$$

Some possible chemical reactions of the reactants involved in the etching process are

$$2H_2O_2(l) \Leftrightarrow 2H_2O(l) + O_2(g), \tag{5.4}$$

$$H_3PO_4(l) + 3H_2O(l) \Leftrightarrow PO_4^{3-}(l) + 3H_3O^+(l). \tag{5.5}$$

During the surface reaction

$$2M_2(s) + 2H_2O_2(l) + 4H_3PO_4(l) + 2O_2(g) + 12H_2O(l)$$

$$\Leftrightarrow 4M_3^+(l) + 4PO_4^{3-}(l) + 12H_3O^+(l) + 6O^{2-}(l) + 2H_2O(l). \quad (5.6)$$

Meanwhile, the chemical reaction for the etched products can be expressed as:

$$2M_2(s) + 2H_2O_2(l) + 4H_3PO_4(l) + 2O_2(g) + 12H_2O(l)$$

$$\Leftrightarrow 4M_3^+(l) + 4PO_4^{3-}(l) + 12H_3O^+(l) + 6O^{2-}(l) + 2H_2O(l)$$

$$\Leftrightarrow 2MPO_4(s) + M_2O_3(s) + 2PO_4^{3-}(l) + 6H_3O^+(l) + 11H_2O(l). \quad (5.7)$$

After that, water helps to transport the soluble etched product away from the semiconductor surface. The sequence of wet etch process are summarized in Fig. 5.1.

5.2.2 Experimental Details of InAs Wet Etching

InAs substrates with surface orientation of (001), (110), (111)A, and (111)B were used for the wet etch experiments. The substrates have n-type doping concentration (N_D) of 1×10^{17} cm^{-3}. The process flow for anisotropic wet etch of InAs is shown in Fig. 5.2. First, photoresist is spin-coated at 3000 rotation per minute on the InAs substrate as shown in Fig. 5.2 (a). Next, the InAs sample is secured on a sample holder. This is followed by patterning of rectangular-shaped etch mask windows with different in-plane orientation (θ) on the InAs substrates by rotating the sample holder as illustrated in Fig. 5.2 (b). In Fig. 5.2 (c), the photoresist is developed and subsequently hard baked for 10 minutes at 110 °C. H_3PO_4:H_2O_2:H_2O solution (1:5:20 by volume) was then used to etch the patterned substrates at room temperature. Finally, the photoresist is striped using O_2-based plasma at 180 °C for 10 minutes.

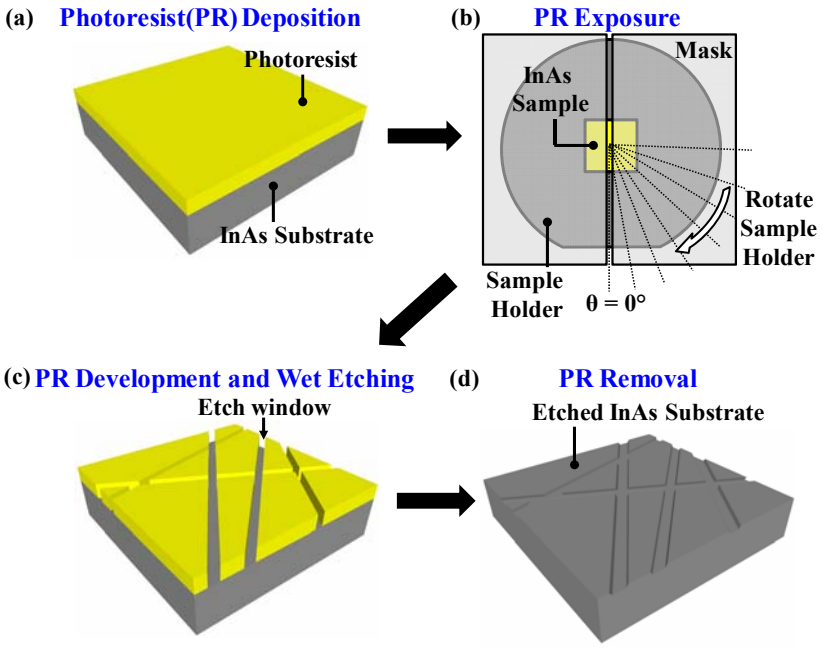


Fig. 5.2 Schematic showing the process flow for anisotropic wet etch of InAs. The key steps include (a) photoresist deposition, (b) photoresist exposure, (c) photoresist development followed by wet etch process, and (d) photoresist removal.

In InAs, a free (111)A surface has one In atom attached firmly to three As atoms underneath it so that the valency of 3 is completely satisfied. The (111)B plane contains As atoms that have two extra unbounded electron per atom owing to its valency of 5 [172]-[174]. Since oxidation involves loss of electrons, the As atoms present on a (111)B surface react much more readily with the oxidizer than In atoms on a (111)A surface. Once As atoms at the (111)B surface is removed by oxidation, the underlying In atoms are dislodged easily by the oxidation process. Consequently, the (111)B etch rate is found to be the highest in InAs for reaction-rate limited etching process. Meanwhile, the ideal (001) surface also has either group-III or group-V terminated surface. However, the polar (001) surfaces often undergone surface reconstruction for sample prepared by different condition, each with different surface coverage of group-V (or group-III) atom [169]]. This suggest that the reactivity of (001) surface could be ranging from (111)B to slightly higher than (111)A. For (110) plane, the surface consists of equal numbers of

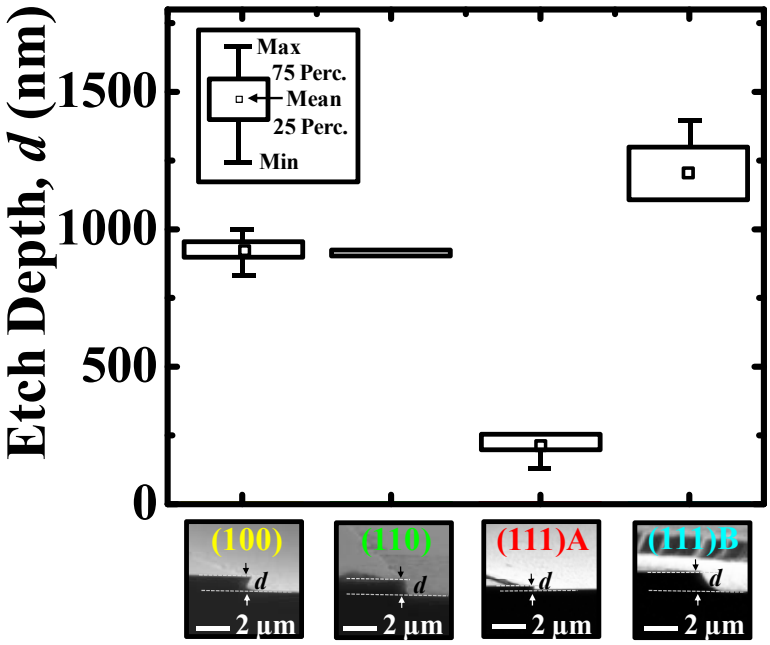


Fig. 5.3 Box-plot showing etch depth of InAs having (001), (110), (111)A and (111)B surface orientations after etching in H_3PO_4:H_2O_2:H_2O (1:5:20 by volume) solution for 2 minutes. The (001):(110):(111)A:(111)B etch rate ratio is found to be 4:4.2:1:5.5.

each of the constituent atoms. Hence, this suggest that the reactivity lies in between (111)A and (111)B. In our experiment, the etch rate of both (001) and (110) surface are comparable and lies in between (111)A and (111)B. Fig. 5.3 shows the etch depth as a function of InAs crystal orientation. The etch rate ratio of (001):(110):(111)A:(111)B in our experiment is found to be 4:4.2:1:5.5.

5.2.3 Theoretical Prediction of 3D Etch Profile of InAs

Due to preferential etching of certain crystallographic planes in III-V materials, the resultant wet etch profile of III-V material will be faceted and bound by the crystallographic planes with low etch rates, as predicted by Wulff theory [175]. In this Section, we present a

physical model based on geometrical constructions to predict the 3-dimensional (3D) etch profiles of InAs on different substrate orientations using (001), (110), (111)A and (111)B as limiting facets as shown in Fig. 5.4.

To construct the 3D etch profile of InAs, we first consider the 3D shape bounded by each (001), (110), (111)A and (111)B crystallographic planes on various substrate orientations, respectively. The 3D shape bounded by (001) crystallographic planes resembles a cuboid. (110) crystallographic planes resemble a rhombic dodecahedron. (111)A crystallographic planes resemble a tetrahedron. (111)B crystallographic planes resemble an inverted tetrahedron. These polyhedrons are illustrated in Fig. 5.4 (a). The relative size of these polyhedrons are proportional to their etch rate and etch time (t).

The theoretical prediction of the 3D etch profile for InAs is the smallest 3D shape bounded by all the polyhedrons as shown in Fig. 5.4 (b). Evolutions of the theoretically predicted InAs 3D etch profile with t on different substrate orientations are shown in Fig. 5.4 (c). In the order from left to right, the InAs 3D etch profiles represent the initial, intermediate, and final stage of wet etch process. In our model, the InAs 3D etch profile at the initial stage is not stable and constantly evolving. During intermediate stage of etching, the InAs 3D etch profile is meta-stable, and remains relatively unchanged for

$$t < \frac{W\{\sin[\alpha_{(ijk)}]\}}{r_{(hkl)}}, \tag{5.8}$$

where W is the width of etch mask opening, (ijk) is the crystallographic plane with lowest etch rate, $\alpha_{(ijk)}$ is the facet angle between the (ijk) crystallographic plane and the substrate surface, (hkl) is the substrate's orientation, and $r_{(hkl)}$ is the etch rate of the (hkl) substrate. During intermediate etching stage, any arbitrary (lmn) crystallographic planes with etch rate

$$r_{(lmn)} < \frac{r_{(hkl)} + r_{(ijk)}}{\{\sin[\alpha_{(ijk)}]\}^2} + r_{(ijk)} \sin[\alpha_{(lmn)}] \ , \tag{5.9}$$

could be present along with the crystallographic plane with the lowest etch rate. In equation (5.9), $r_{(ijk)}$ is the etch rate of the crystallographic plane with the lowest etch rate and $\alpha_{(lmn)}$ is the facet angle between the (lmn) oriented crystallographic plane and the substrate surface. At the final etching stage where

$$t >> \frac{W\{\sin[\alpha_{(ijk)}]\}}{r_{(hkl)}}, \tag{5.10}$$

only the crystallographic plane with the slowest etch rate remains.

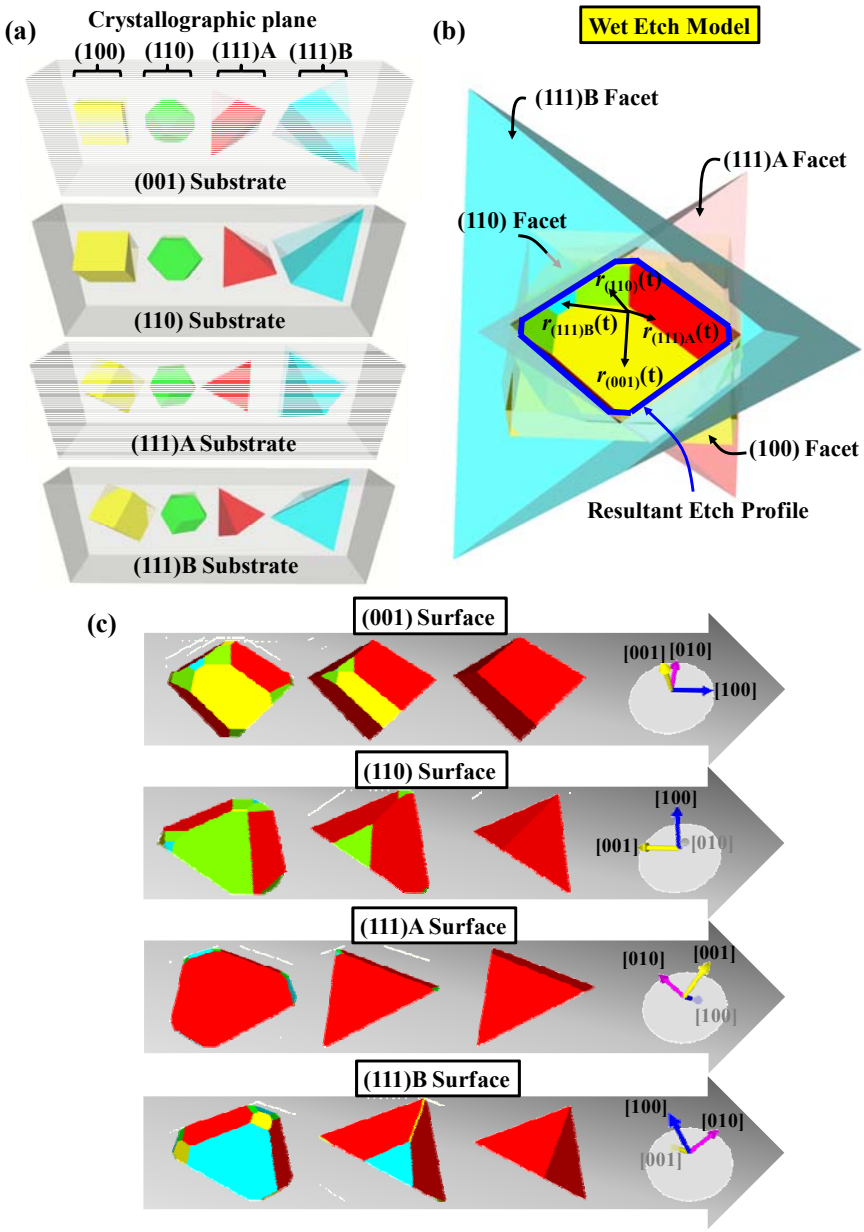


Fig. 5.4 Schematics of (a) 3D shape bounded by (001), (110), (111)A, and (111)B crystallographic planes on (001), (110), (111)A, and (111)B substrates, respectively. (b) The theoretical prediction of 3D etch profile for InAs is the smallest 3D shape enclosed by the (001), (110), (111)A, and (111)B polyhedrons. (c) Evolution the theoretically predicted 3D etch profile for InAs with etch time.

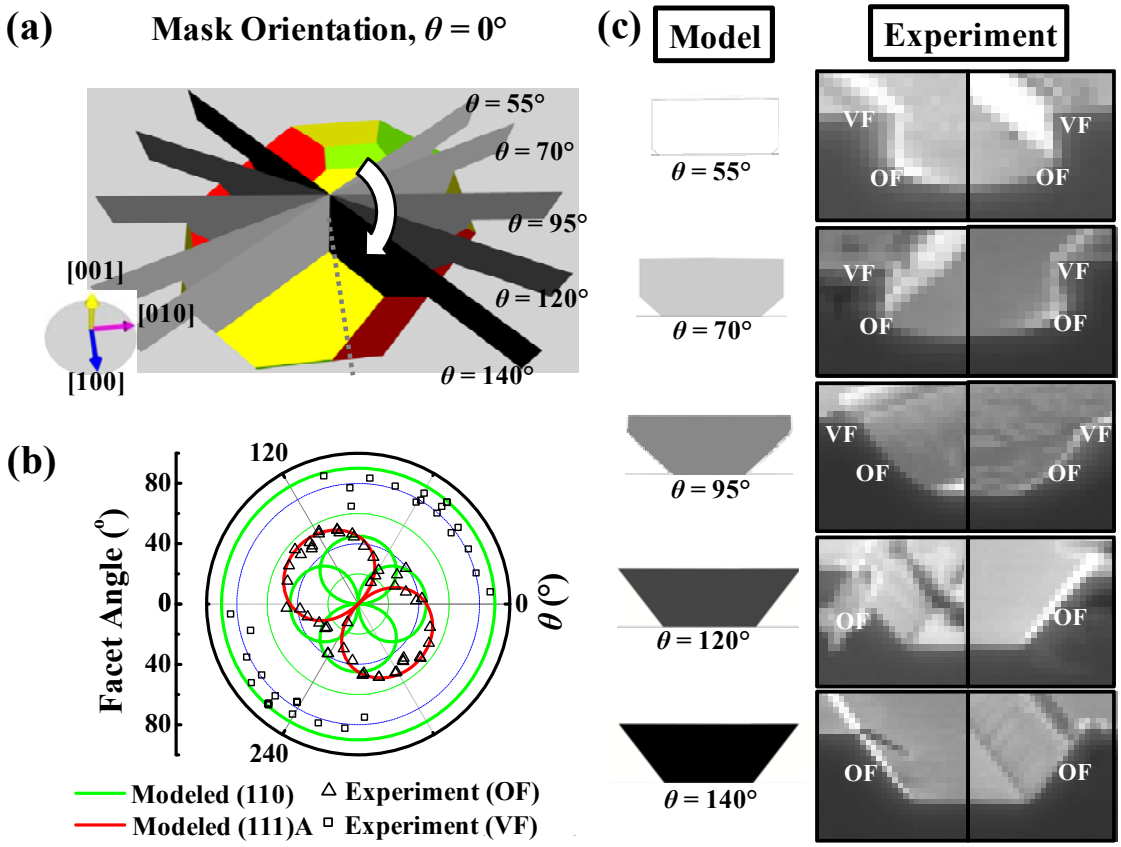


Fig. 5.5 (a) Schematic showing theoretical 3D etch profile on the (001) InAs substrate. (b) Polar plot of the lateral undercut facet angle as a function of etch mask orientation θ. Open symbols represent experimentally measured facet angles. Green and red lines represent the modeled facet angles bounded by (110) and (111)A crystallographic planes, respectively. (c) Schematics of the modeled cross sectional etch profiles (left column) and scanning electron microscopy (SEM) images of the experimental etch profiles (right column) at θ of 55 °, 70 °, 95 °, 120 °, and 140 ° showing excellent agreement.

5.2.4 3D Etch Profile on (001) InAs Substrate

The 3D etch profile on (001) InAs substrate is bounded by (001), (110) and (111)A crystallographic planes, as shown in Fig. 5.5 (a). In Fig. 5.45 (b), a polar plot for the modeled and experimental measured facet angles as a function of θ is shown. The experimental lateral undercut profiles were predominantly outward facing facets (OF) and vertical facets (VF). We

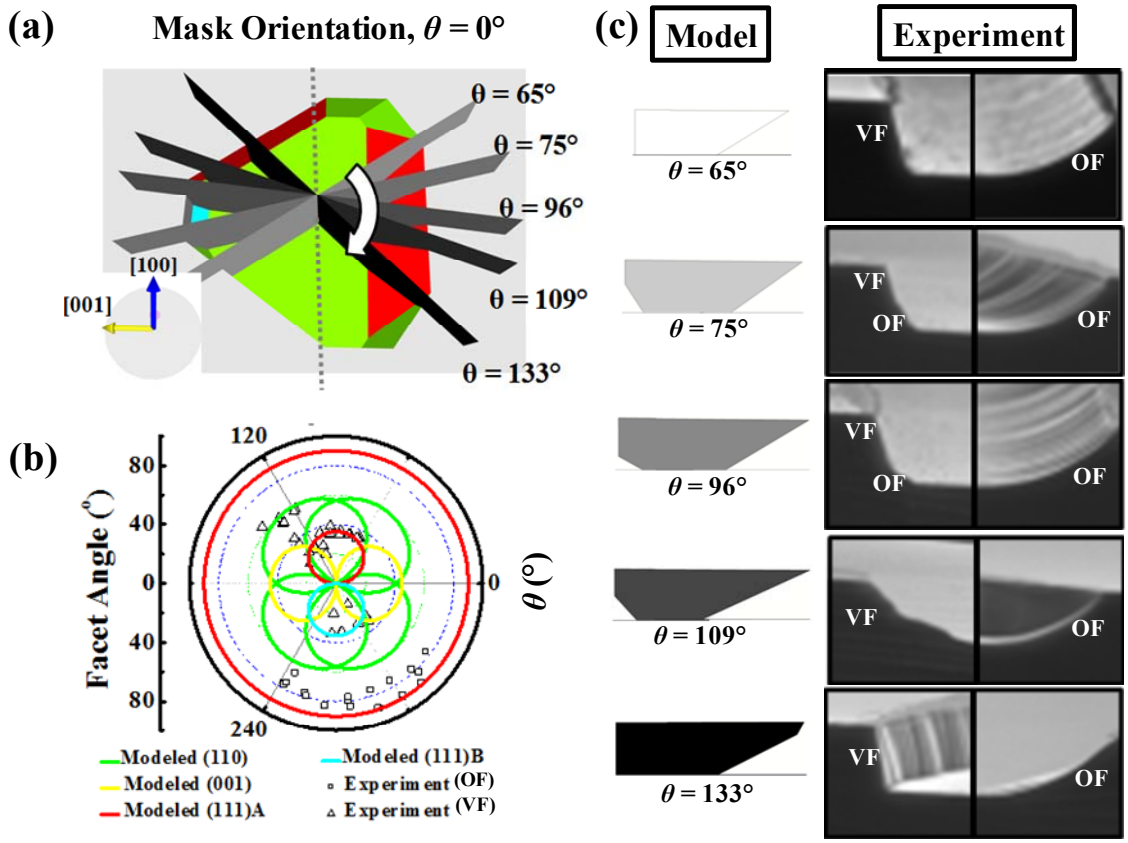


Fig. 5.6 (a) Schematic showing theoretical 3D etch profile on the (110) InAs substrate. (b) Polar plot of the lateral undercut facet angle as a function of θ. Open symbols represent experimentally measured facet angles. Yellow, green, red, and blue lines represent the modeled facet angles bounded by (001), (110), (111)A, and (111)B crystallographic planes, respectively. (c) Schematics of the modeled cross sectional etch profiles (left column) and SEM images of the experimental etch profiles (right column) at θ of 65 °, 75 °, 96 °, 109 °, and 133 ° showing good agreement.

found that these facets type and their respective facet angles correspond to the modeled (110) and (111)A crystallographic planes. In Fig. 5.5 (c), we show that our modeled lateral undercut profiles at θ of 55 °, 70 °, 95 °, 120 °, and 140 ° agree well with the experimental results. The modeled cross sections of the etch profile were obtained by intersecting planes which are orthogonal to their respective θ with the theoretical 3D etch profile.

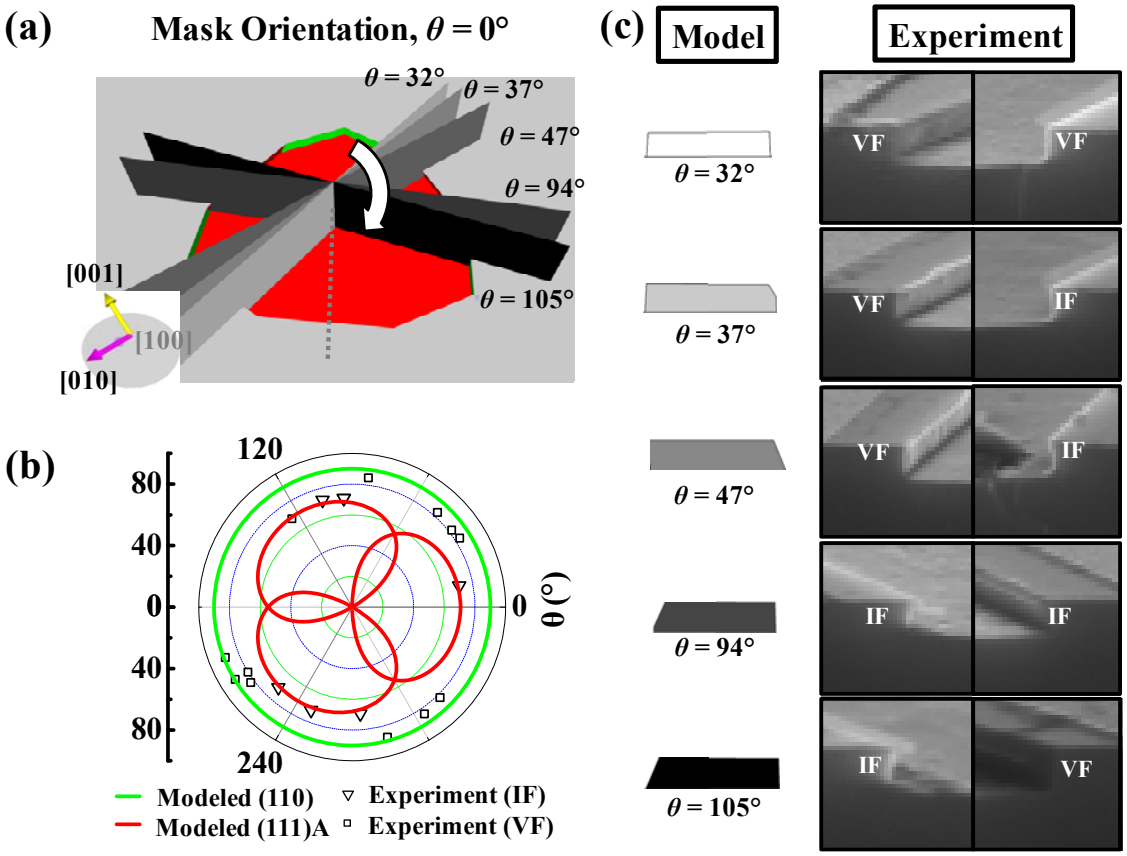


Fig. 5.7 (a) Schematic showing theoretical 3D etch profile on the (111)A InAs substrate. (b) Polar plot of the lateral undercut facet angle as a function of θ. Open symbols represent experimentally measured facet angles. Green and red lines represent the modeled facet angles bounded by (110) and (111)A crystallographic planes, respectively. (c) Schematics of the modeled cross sectional etch profiles (left column) and SEM images of the experimental etch profiles (right column) at θ of 32 °, 37 °, 47 °, 94 °, and 105 ° showing good agreement.

5.2.5 3D Etch Profile on (110) InAs Substrate

The 3D etch profile on (110) InAs substrate is bounded by (001), (110), (111)A and (111)B crystallographic planes as shown in Fig. 5.6 (a). The experimental lateral undercut profiles were predominantly OF and VF. We found that these facets type and their respective facet angles correspond to the modeled (001), (110), (111)A and (111)B crystallographic planes,

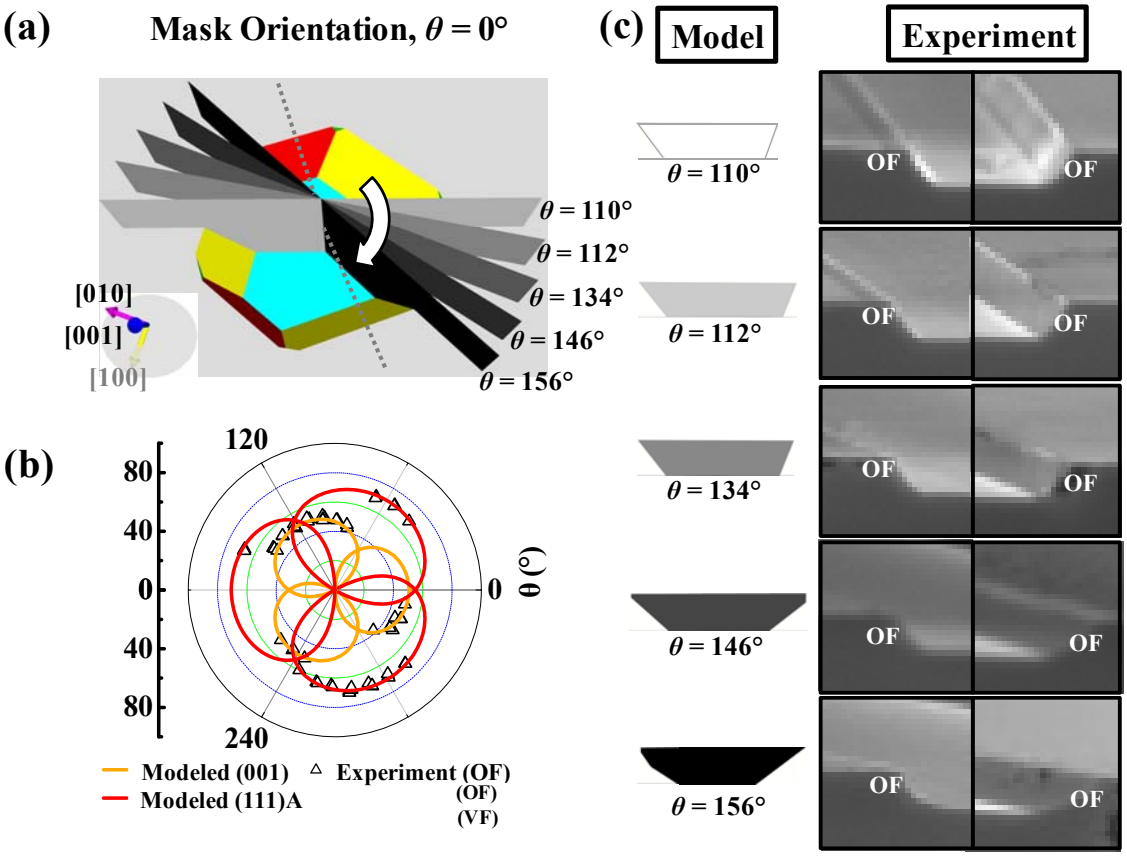


Fig. 5.8 (a) Schematic showing theoretical 3D etch profile on the (111)B InAs substrate. (b) Polar plot of the lateral undercut facet angle as a function of θ. Open symbols represent experimentally measured facet angles. Yellow and red lines represent the modeled facet angles bounded by (001) and (111)A crystallographic planes, respectively. (c) Schematics of the modeled cross-sectional etch profiles (left column) and SEM images of the experimental etch profiles (right column) at θ of 110 °, 122 °, 134 °, 146 °, and 156 ° showing good agreement.

as shown in Fig. 5.6 (b). In Fig. 5.6 (c), we show that our modeled lateral undercut profiles at θ of 65 °, 75 °, 96 °, 109 °, and 133 ° agree well with the experimental results.

5.2.6 3D Etch Profile on (111)A InAs Substrate

The 3D etch profile on (111)A InAs substrate is bounded by (110) and (111)A crystallographic planes, as shown in Fig. 5.7 (a). The experimental lateral undercut profiles were

predominantly inward facing facets (IF) and VF. We found that these facets type and their respective facet angles correspond to the modeled (110) and (111)A crystallographic planes, as shown in Fig. 5.7 (b). In Fig. 5.7 (c), we show that our modeled lateral undercut profiles at θ of 32 °, 37 °, 47 °, 94 °, and 105 ° agree well with the experimental results.

. 3D Etch Profile on (111)B InAs Substrate

The 3D etching shape on (111)B InAs substrate is bounded by (001) and (111)A crystallographic planes, as shown in Fig. 5.8 (a). Only OF lateral undercut profile was present. The experimentally measured facet angles correspond to the modeled (001) and (111)A crystallographic planes, as shown in Fig. 5.8 (b). In Fig. 5.8 (c), we show that our modeled lateral undercut profile at θ of 110 °, 122 °, 134 °, 146 °, and 156 ° agree well with the experimental results.

In the case of (001), (111)A and (111)B, etching of InAs in H_3PO_4:H_2O_2:H_2O (1:5:20 by volume) yield a rather smooth sidewall profile, as shown in Fig. 5.5, Fig. 5.7 and Fig. 5.8. This is a characteristics of an anisotropic wet etch profile, as the line-edge roughness of the etch mask could be "smoothen out" due to the preferential etching on certain planes. On the other hand, the etch profile on (110) sidewall surface is rather coarse. This could be due to the pattern transfer from the line-edge roughness of the masking layer due to the isotropic nature of the InAs (110) etch in H_3PO_4:H_2O_2:H_2O (1:5:20 by volume).

In summary, our wet etch study provides a qualitative description for the anisotropic wet etch profile for various experimental lateral undercut profiles with different θ on (001), (110), (111)A, and (111)B substrate. It should be noted however that some of the wet etch profiles, particularly on InAs(110) are rather isotropic in nature. This suggest that the etching of InAs(110) using H_3PO_4:H_2O_2:H_2O (1:5:20 by volume) are in diffusion limited regime. Further calibration of the etching conditions need to be carried out in order to verify the geometrical

modeling. The crucial findings in this Section is that the etch profile found on (001) InAs surface along [110] and $[1\bar{1}0]$orientation can be exploited for the realization of novel device structures, which will be demonstrated in the following Sections.

5.3 InGaAs Nanowire nFET with Tapered S/D Structure

5.3.1 Design Concept

The 3D schematic of a novel short-channel junctionless NW nFET is shown in Fig. 5.9 (a). The key features of the device lie in its unique geometry, namely the closely-spaced OF etch profiles (V-Groove) along $[1\bar{1}0]$ orientation and IF etch profiles (Dove-Tail) along [110] orientation on the (001) $In_{0.53}Ga_{0.47}As$ substrate. The V-Groove etch profile enables the realization of NWFETs with ultra-short

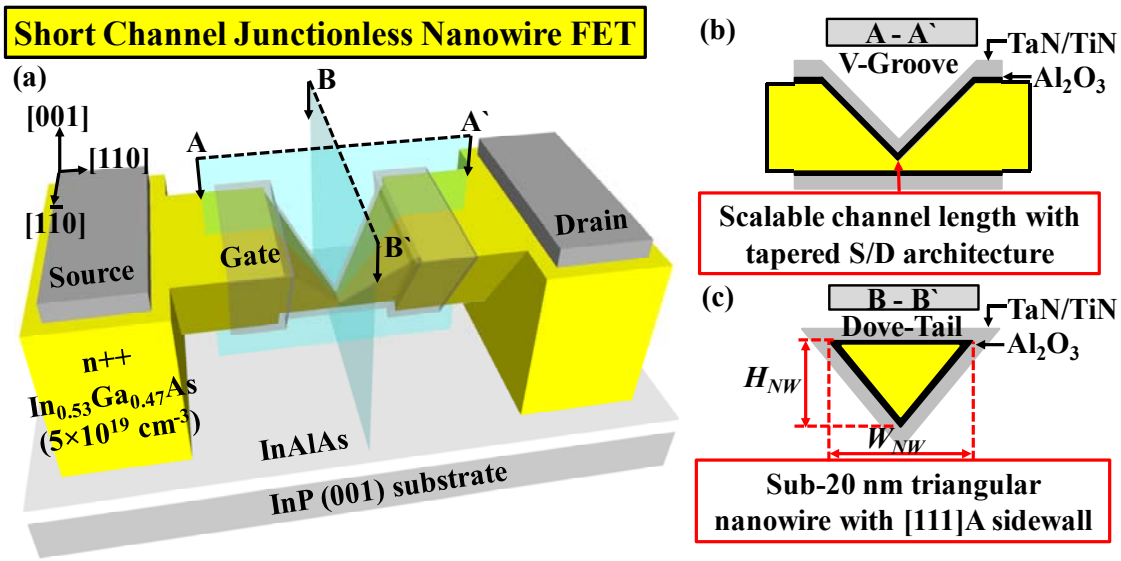


Fig. 5.9 (a) Schematic of a novel short channel $In_{0.53}Ga_{0.47}As$ junctionless nanowire FET structure featuring (b) a scalable channel length with raised S/D structure and (c) a sub-20 nm triangular nanowire with [111]A sidewall.

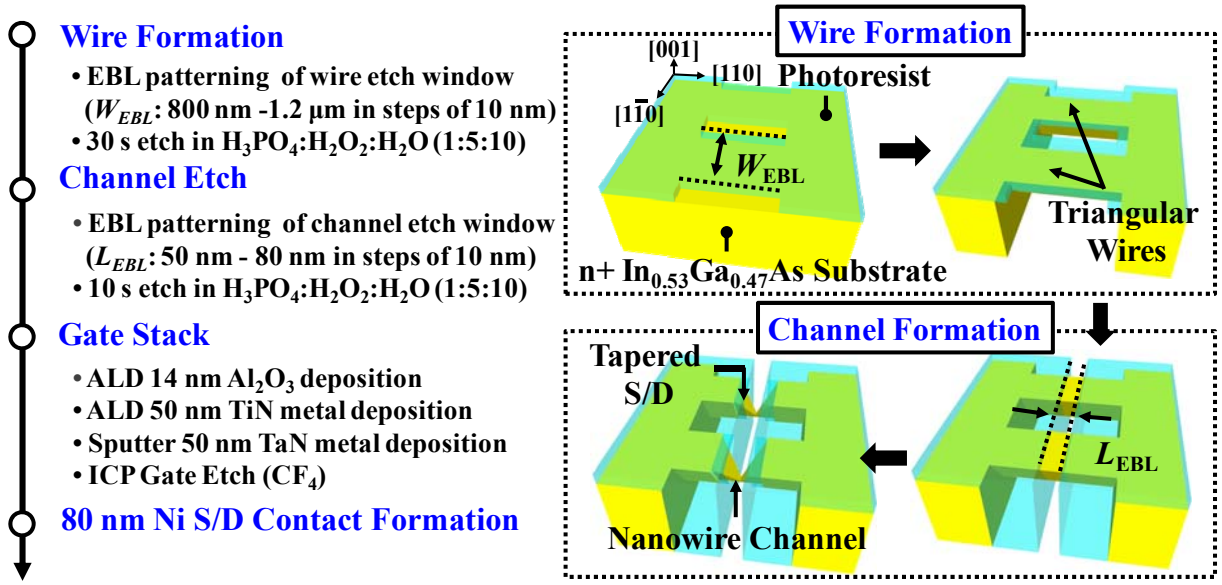


Fig. 5.10 Process flow for fabricating short channel JL-NWFETs with tapered S/D. The schematics illustrate the formation of NWs with triangular cross-section using the Dove-Tail profile followed by the formation of tapered S/D nanowire using the V-Groove profile.

L_{CH} down to sub 20 nm and a tapered S/D structure for achieving low resistance in the NW S/D extension region (R_{EXT}), as shown in Fig. 5.9 (b). In Fig. 5.9 (c), the Dove-Tail etch profile forms NWs with triangular cross-section and exposes the $In_{0.53}Ga_{0.47}As$ [111]A NW sidewall surface which has low density of interface traps (D_{it}) [108]-[109] for good semiconductor-dielectric interface. Furthermore, a very small NW width (W_{NW}) down to sub-20 nm can be realized by optimizing the process for V-Groove and Dove-Tail formations to control SCEs. In addition, the NW formation process is implant-free and damage-free by dry etch for high carrier mobility.

5.3.2 Fabrication of Short-Channel $In_{0.53}Ga_{0.47}As$ Junctionless Nanowire nFETs (JL-NWFETs) with Tapered S/D Structure

Fig. 5.10 shows the process flow for fabricating $In_{0.53}Ga_{0.47}As$ JL-NWFETs structure with tapered S/D structure. The starting substrate comprises of a 250 nm thick heavily-doped n^{++} (doping level N_D of 5×10^{19} cm^{-3}) $In_{0.53}Ga_{0.47}As$ with a 30 nm thick InAlAs barrier layer on

the bulk InP (001) substrate. The substrate was purchased from IntelliEPI and the epi-layers are grown by molecular beam epitaxy (MBE) method. First, etch windows with size of 1 μm × 1 μm and orientation along the [110] direction were defined by electron beam lithography (EBL). Spacing between these etch windows (W_{EBL}) range from 0.8 to 1.2 μm.

Anisotropic wet etch of n^{++} $In_{0.53}Ga_{0.47}As$ using H_3PO_4:H_2O_2:H_2O (1:5:20 by volume) solution was then performed for 30 s at room temperature. Anisotropic wet etch of n^{++} $In_{0.53}Ga_{0.47}As$ through the etch window resulted in the Dove-Tail profile as illustrated in Fig. 5.11 (a) and formed [110]-oriented wires with triangular cross-section and (111)A Ga-terminated surface, as shown in Fig. 5.11 (b). Rectangular-shaped etch windows with the opening size (L_{EBL}) ranging from 50 to 80 nm were then aligned to the wires along the $[1\bar{1}0]$ direction. This was followed by an anisotropic wet etch in H_3PO_4:H_2O_2:H_2O (1:5:20 by volume) for 10 s at

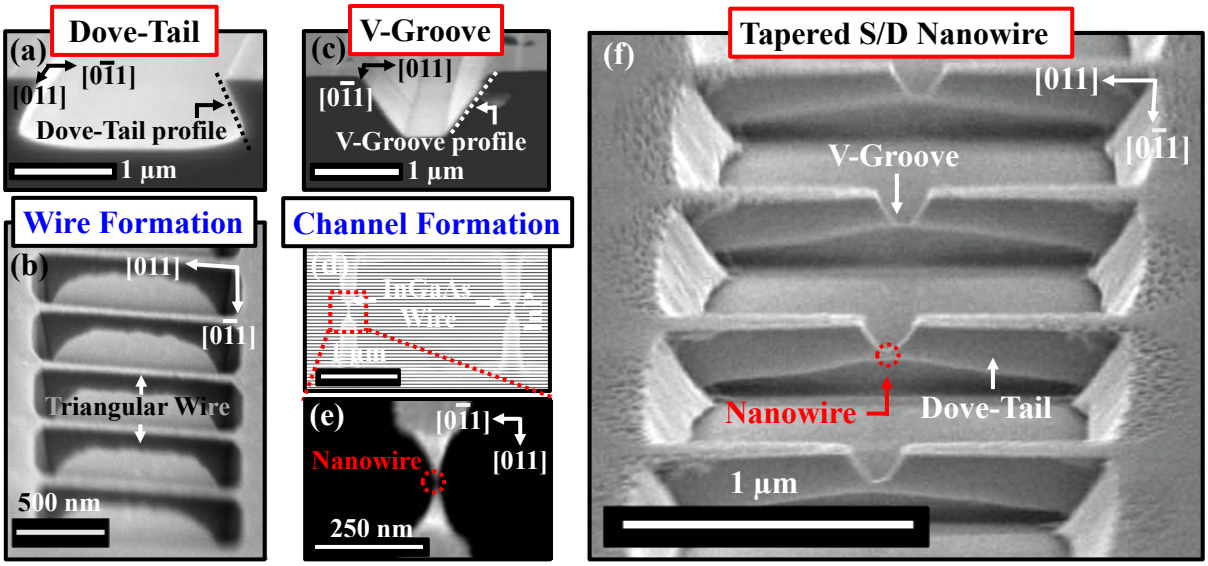


Fig. 5.11 (a) Tilted SEM view of Dove-Tail etch profile along [011] edge. (b) Tilted SEM view of [011] oriented triangular wires formed by anisotropic wet etch, (c) Tilted SEM view of V-Groove etch profile along $[1\bar{1}0]$ edge. (d) Top SEM view of tapered S/D NWs. (e) Zoomed in SEM view on the NW channel, and (f) tilted SEM view of the tapered S/D nanowire, showing that a short-channel NWs with small A_{NW} was achieved at the intersection between V-Groove and Dove-Tail etch profiles.

room temperature, resulting in the formation of the V-Groove profile as shown in Fig. 5.11 (c). This defines the L_{CH} and tapered S/D structure of the NW as illustrated in Fig. 5.11 (d). In Fig. 5.11 (e)-(f), short-channel JL-NWFETs with small NW cross-sectional area (A_{NW}) were achieved at the intersection between V-Groove and Dove-Tail. The L_{CH} and the W_{NW} can be engineered by carefully optimizing the W_{EBL}, L_{EBL}, and t.

After the NW formation, the gate stack was formed by depositing 14 nm-thick Al2O3 using atomic layer deposition (ALD). This was followed by the deposition of 50 nm-thick ALD TiN layer with conformal coverage over the NW channel. 50 nm-thick TaN metal gate was then sputter-deposited. Finally, Ohmic contact was formed by depositing 80 nm-thick Ni in the S/D region to complete the device fabrication. The layout used for the fabrication of NWFETs with tapered S/D can be found in Appendix 5.6.1.

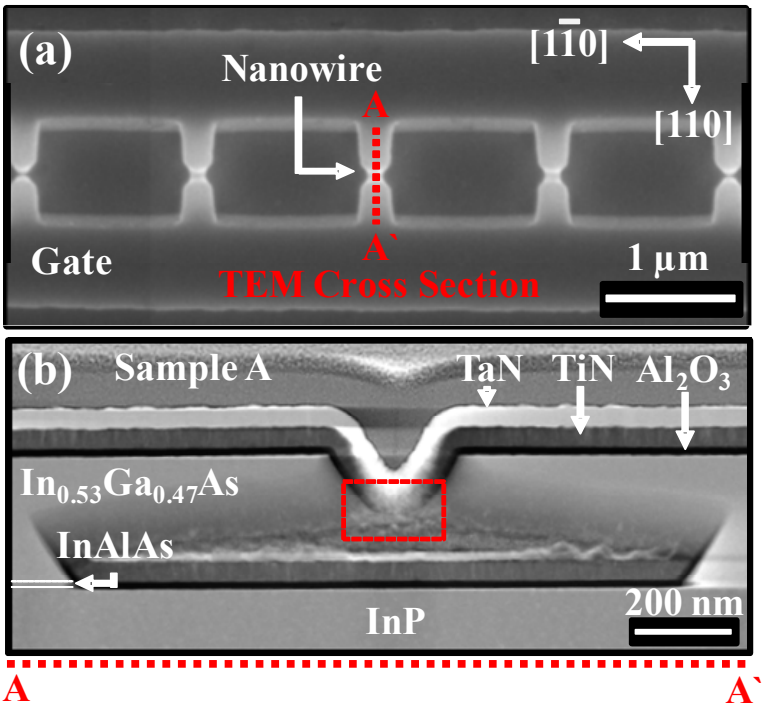


Fig. 5.12 (a) Top-view SEM image of the nanowire after the gate stack formation. FIB cut was performed along A-A` (b) Cross-sectional HAADF-STEM image along A-A' showing the channel of the JL-NWFETs.

5.3.3 Physical and Electrical Characterization of JL-NWFETs

The top-view SEM image of a completed transistor is shown in Fig. 5.12 (a). The cross-sectional high-angle annular dark field scanning transmission electron microscope (HAADF-TEM) image taken along A-A` in Fig. 5.12 (b) shows the channel region of a $In_{0.53}Ga_{0.47}As$ JL-NWFET device with the TaN/TiN/Al_2O_3 gate stack and raised S/D structure. Zoom-in TEM view (bright field) of the nanowire region in Fig. 5.13 shows that the {111}A, {113}A and {100} facets are present. L_{CH} of 20 nm and nanowire height (H_{NW}) of 15 nm was achieved for device A [Fig. 5.12 (a)] and L_{CH} of 14 nm and H_{NW} of 15 nm was achieved for device B [Fig. 5.12 (b)]. The zone axis (ZA) for the HRTEM images is $[0\bar{1}1]$.

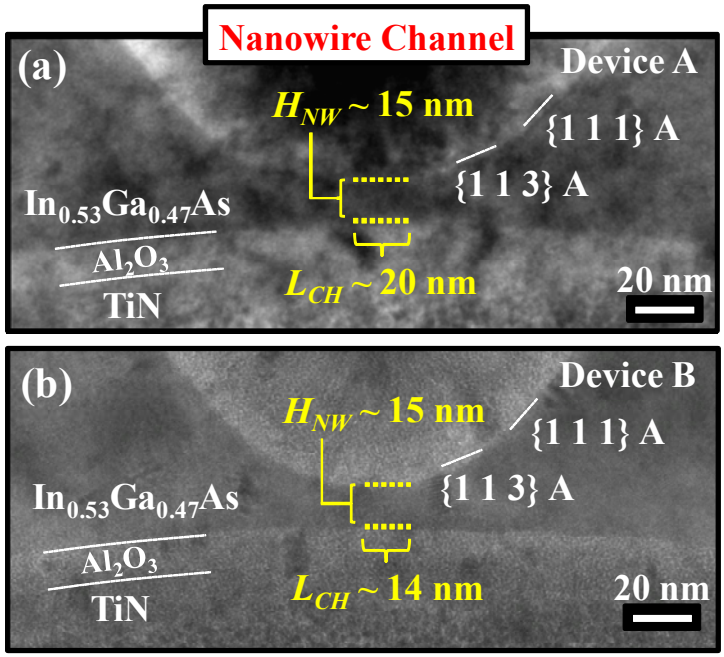


Fig. 5.13 Cross-sectional TEM image (bright-field) of (a) device A showing L_{CH} of 20 nm and H_{NW} of 15 nm and (b) device B with L_{CH} of 14 nm and H_{NW} of 15 nm. The zone-axis of the TEM image is [110]. The TEM was performed at Data Storage Institute (DSI) through a service contract. The ZA of the HRTEM image is $[0\bar{1}1]$.

Fig. 5.14 to Fig. 5.16 show the well-behaved I_D versus gate voltage (V_G), transconductance (G_M) versus V_G, and I_D versus drain voltage (V_D) characteristics of the devices shown in Fig. 5.12 (device A and device B). The I_D and G_M were normalized to the perimeter (W_G) = 2 × [tan(35.3) + sec(35.3)] × H_{NW} × (wire number). The JL-NWFET device with 20 nm L_{CH} and 15 nm H_{NW} shows good *SS* of 150 mV/decade, indicating excellent gate electrostatic control by the gate-all-around (GAA) structure despite a very large effective oxide thickness (EOT) of ~6 nm. Further suppression of SCEs can be achieved by scaling down the EOT and N_D reduction. The NW device operates in the depletion-mode with threshold voltage (V_T) of -0.5 V, extracted by linear extrapolation at V_D of 0.05 V. At V_D of 0.5 V, the device with 14 nm L_{CH}

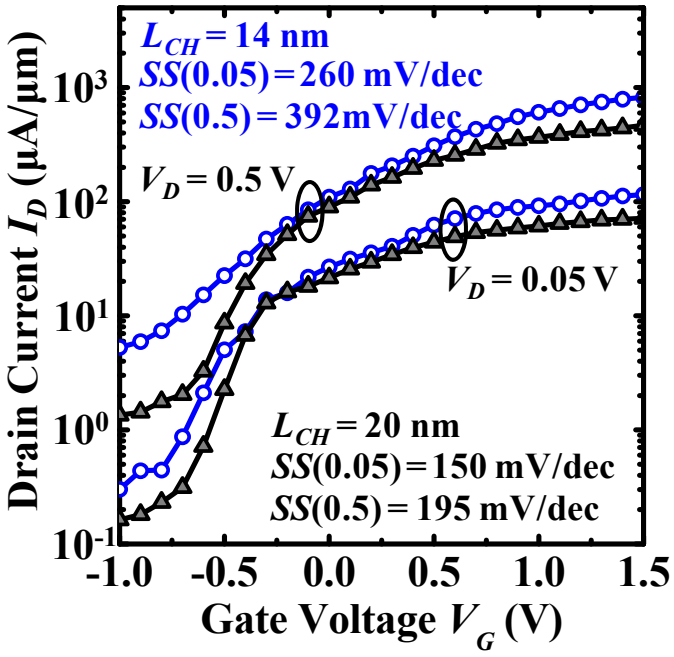


Fig. 5.14 I_D-V_G of the JL-NWFETs (device A and device B) normalized to perimeter. NWFET with L_{CH} of 20 nm (device B) achieved small *SS* of 195 mV/decade at V_D of 0.5 V and *DIBL* of 260 mV/decade despite having large EOT of 6 nm and N_D of 5×10^{19} cm^{-3}.

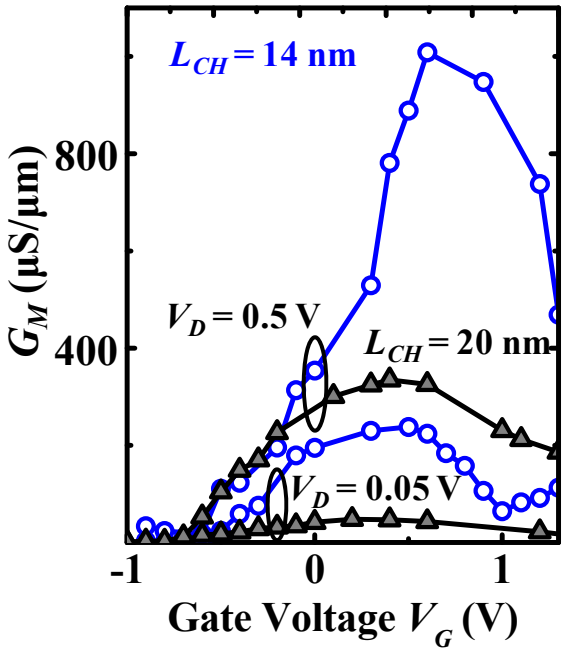


Fig. 5.15 Extrinsic Transconductance G_M-V_G of the JL-NWFETs (device A and device B). The JL-NWFET with 14 nm L_{CH} achieves $G_{M,peak}$ of 1000 μS/μm at V_D of 0.5 V.

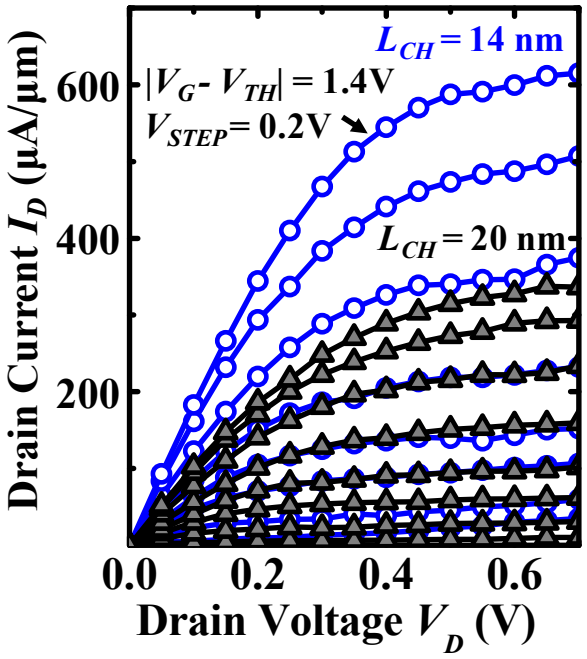
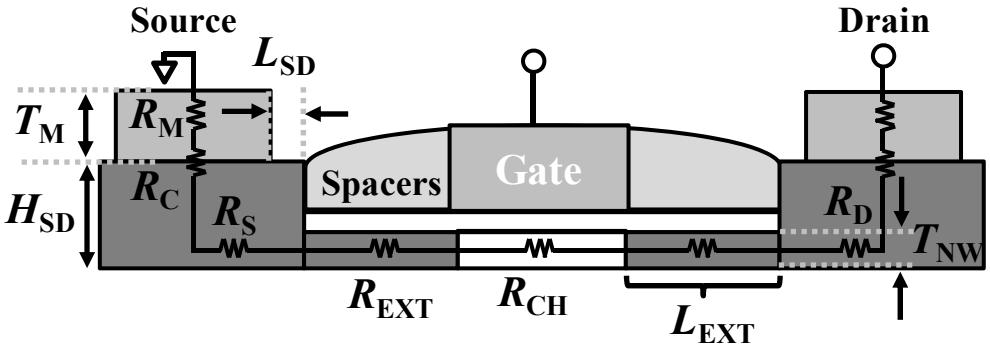


Fig. 5.16 Output characteristics of the JL-NWFETs (device A and device B). Drive current of 14 nm L_{CH} device is ~200 μA/μm at the gate overdrive of 0.5 V and V_D of 0.5 V.



$$R_T = 2(R_M + R_C) + R_S + R_D + 2R_{EXT} + R_{CH}$$

Fig. 5.17 Schematic showing the resistance components of a typical NWFET. They include metak resistance (R_M), contact resistance (R_C), source resistance (R_S), drain resistance (R_D), $R_{EXT,}$ and channel resistance (R_{CH}). R_{EXT} contribute to a significant part of the total resistance (R_T) due to its small A_{NW}.

delivered peak extrinsic transconductance ($G_{M,peak}$) of 1000 μS/μm as shown in Fig. 5.15. Drive current of 200 μA/μm was achieved at gate over drive of 0.5 V and V_D of 0.5 V, as shown in the output characteristics of the same device in Fig. 5.16.

Various resistance components of the JL-NWFET are shown in Fig. 5.17. The total resistance (R_T) comprises of channel resistance (R_{CH}), R_{EXT}, source resistance (R_S), drain resistance (R_D), contact resistance between semiconductor and metal contact (R_C), and metal resistance (R_M). In NWFET, a significant component of R_T is R_{EXT} due to the small A_{NW}.

Due to the tapered S/D structure in our novel device architecture, R_{EXT} can be drastically reduced as compared to NWFETs without raised S/D structure. The plot of R_T in the linear regime (V_D = 0.05 V) as a function of V_G for the 14 nm L_{CH} NWFET is shown in Fig. 5.18. The curve was fitted using the equation shown in the inset of the Fig. 5.18. The fitted curve was extrapolated to a large V_G of 5 V to obtain the value of R_{SD} which is ~360 Ω·μm. This is among the smallest R_{SD} values reported for InGaAs non-planar structures [150],[161]-[163]. R_{EXT} can be further reduced by employing self-aligned metal S/D technology [46]-[50]. Our results show that NWFET with tapered S/D structure is a

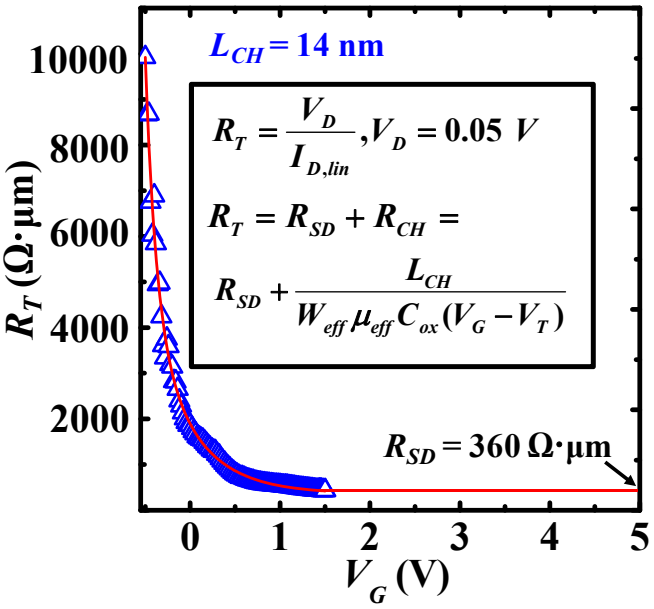


Fig. 5.18 R_T-V_G for the 14 nm L_{CH} JL-NWFET. R_{SD} of 360 Ω·μm is obtained from the extrapolated plot at 5 V. This is among the smallest R_{SD} value reported for InGaAs non-planar structures. In the inset, $I_{D,lin}$ is the drive current in the linear regime, μ_{eff} is the effective carrier mobility, and C_{ox} is the gate oxide capacitance.

promising device design for sustaining the scaling of CMOS to the end-of-roadmap in future low power and high performance logic application.

5.4 Toward Large-Scale Production of Room Temperature Operable SET: Quantum Dots with Self-Aligned S/D Structure

SET is one of the promising device candidates that can possibly complement the functionalities of current CMOS devices for beyond CMOS applications. The basic structure of SET consists of three-terminals: source, drain, and gate. A schematic of SET (Fig. 5.19) is analogous to that of conventional MOSFETs. However, SET has tiny conductive island coupled to gate electrode with gate capacitance (C_G). Source and drain electrodes are connected to the island through a tunnel barrier. The tunnel barrier controls the motion of every single electron. It consists of two conductors separated by the thin insulator layer, and is modeled as source tunneling resistance (R_{TS}), drain tunneling resistance (R_{TD}), source junction capacitance (C_{JS}), and drain junction capacitance (C_{JD}). The gate bias attracts electron to the island through either source or drain tunnel barrier, and the number of electrons on the island only has fixed integer due to "Coulomb blockade" phenomenon. Therefore, the gate bias can control the flow of single electron when a small bias is applied between the source and drain [183],[184].

5.4.1 Design Concept

In this Section, a novel approach to fabricate quantum dots with self-aligned S/D structure is presented, as shown in Fig 5.20. This architecture can be employed to function as a SET. Due to the small cross-sectional area of the S/D adjacent to the quantum dot, the conduction band between the S/D and quantum dot can be modified by the strong quantum

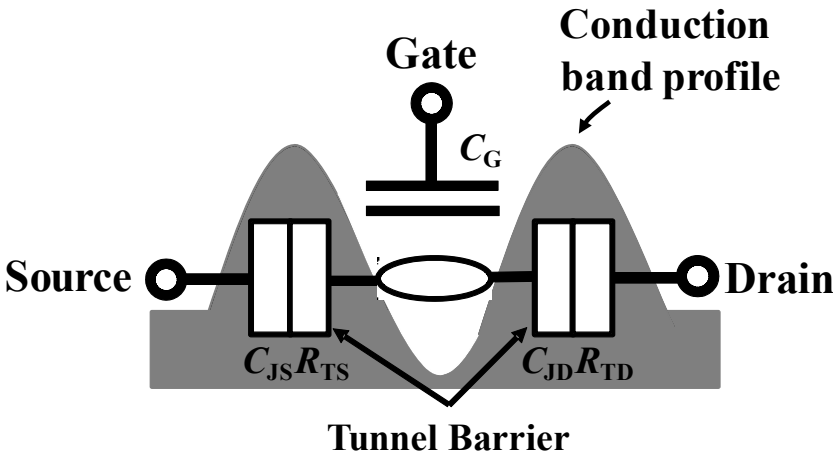


Fig. 5.19 Schematic illustration of a SET. The silhouette represents the conduction band profile of a quantum dot with self-aligned S/D structure.

confinement and behaves as tunnel barrier for electrons. The main features of this novel structure include quantum dots with very small feature size down to sub-30 nm and self-aligned S/D structure as tunnel barrier.

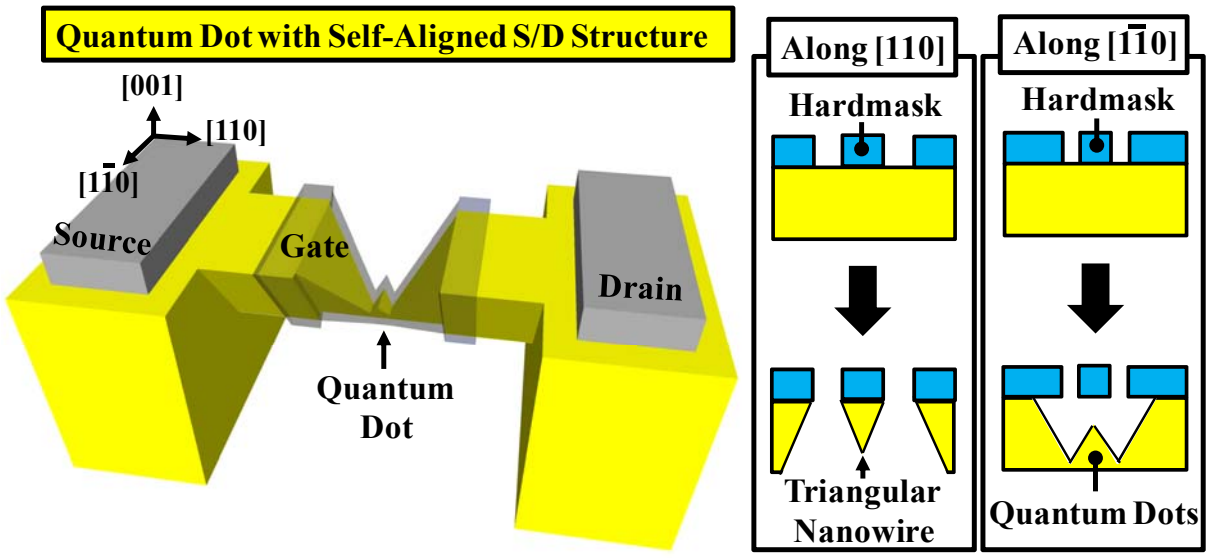


Fig. 5.20 Conceptual schematics of quantum dots with self-aligned S/D realized by two step anisotropic wet etch process. The NW with triangular cross-section is first realized using the Dove-Tail profile along the [110] edge, followed by quantum dot formation using the double V-Groove profiles along the [1$\bar{1}$0] edge.

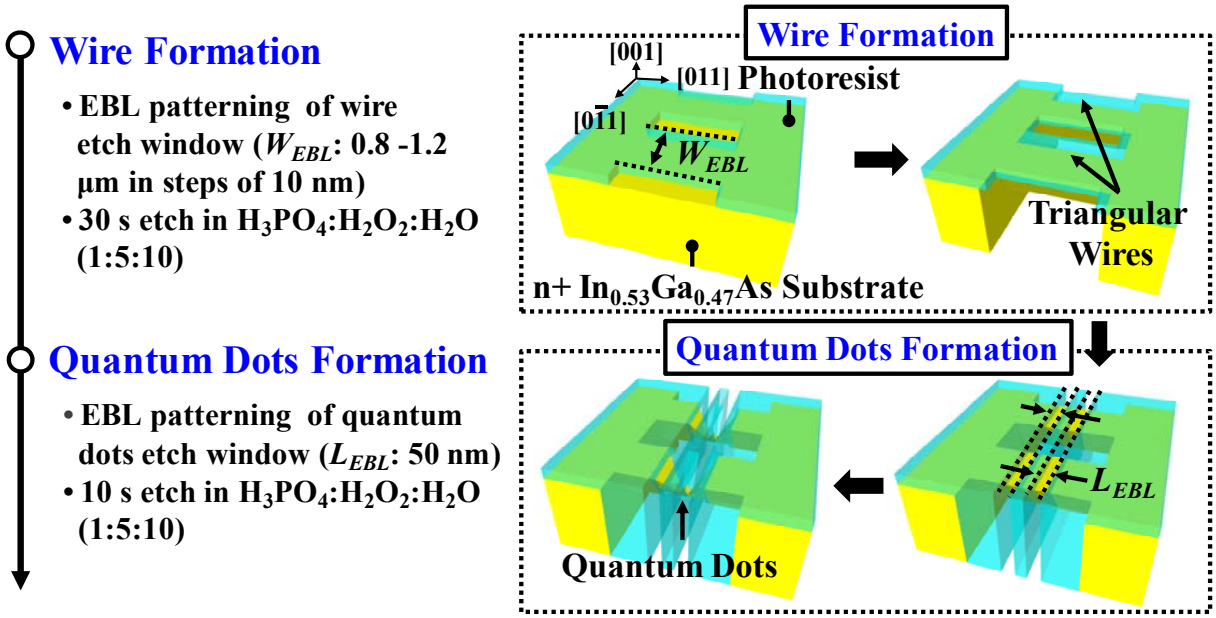


Fig. 5.21 Key fabrication process flow for realizing quantum dot with self-aligned S/D. The schematics show the formation of NWs with triangular cross-section and Dove-Tail profile, and followed by quantum dot formation using double V-Groove etch process.

5.4.2 Fabrication of Quantum Dots with Self-Aligned S/D Structure

Fig. 5.21 shows the key process flow for realizing quantum dots with self-aligned S/D structure. The starting substrate comprises a 250 nm-thick heavily-doped n^{++} $In_{0.53}Ga_{0.47}As$ (5×10^{19} cm^{-3}) with a 30 nm-thick InAlAs barrier layer on bulk InP (001) substrate. First, 1 μm × 1 μm etch windows oriented along the [110] direction with W_{EBL} ranging from 0.8 to 1.2 μm were defined using EBL.

Anisotropic wet etch of n^{++} $In_{0.53}Ga_{0.47}As$ using H_3PO_4:H_2O_2:H_2O (1:5:20 by volume) was then carried out for 30 s. Anisotropic wet etch of n^{++} $In_{0.53}Ga_{0.47}As$ through the etch window resulted in the Dove-Tail profile and formed [110]-oriented triangular wires. Two parallel etch windows were then aligned to the wires along the $[1\bar{1}0]$ direction. The etch windows have L_{EBL}

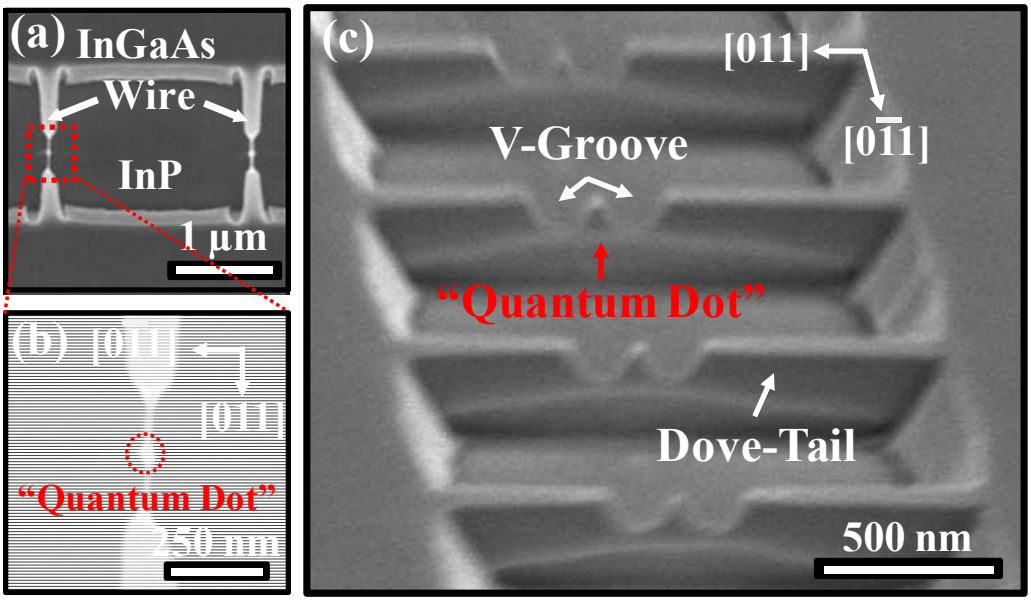


Fig. 5.22 (a) Top-view SEM image of a completed quantum dot with self-aligned S/D structure. (b) Zoom-in view SEM of the quantum dot. Island sizes down to 30-40 nm by 40-60 nm were achieved due to self-limiting etch process. (c) Tilted-view SEM of the quantum dot with self-aligned S/D structure. of 100 nm and spacing (W_{QD}) varying from 20 to 100 nm in step of 5 nm.

This was followed by an anisotropic wet etch in H_3PO_4:H_2O_2:H_2O (1:5:20 by volume) for 10 s. This forms the double V-Grooves profile and defines the quantum dot and the self-aligned S/D structure.

5.4.3 Physical Characterization of the Quantum Dot with Self-aligned S/D Structure

In Fig. 5.22 (a), the top-view of the structure after quantum dot formation step is shown. Zoom-in SEM view in Fig. 5.22 (b) shows that a quantum dot-like structure was obtained at the intersection between the double V-Grooves and the Dove-Tail. Tilt-view SEM in Fig 5.22 (c) shows that a regular tetrahedron-shaped quantum dot structure was achieved.

Our results show that regular tetrahedron-shaped quantum dots with island sizes down to 30-40 nm by 40-60 nm can be achieved by a self-limiting etch process. The quantum dot

dimension is comparable to the island size of a room temperature operable SET device reported in [169]. Smaller quantum dot island size can be achieved with careful calibration of W_{EBL}, $L_{EBL,}$ W_{QD}, and t. To improve the precision of the etching process, a digital etching process can be employed. Our novel and simple fabrication process could pave way for future large scale production of room temperature operable SETs.

5.5 Summary

In this Chapter, we have realized a novel short channel JL-NWFET featuring a tapered S/D architecture. The smallest JL-NWFET has L_{CH} of 14nm and H_{NW} of 15 nm, and exhibits *SS* of 150 mV/decade at V_D of 0.5 V despite a large EOT of 6 nm and substrate doping of 5×10^{19} cm^{-3}. A low R_{SD} of 360 Ω·μm was achieved owing to the unique tapered S/D feature. This is among the lowest R_{SD} reported for InGaAs non-planar structure. Our results show that JL-NWFET with tapered S/D structure is a promising device design candidate for sustaining CMOS scaling to the end-of-roadmap for future low power and high performance logic applications.

Furthermore, we have also developed a novel and simple process for realizing quantum dot with self-aligned S/D structure which could operate as SET. Due to self-limiting etching process, the quantum dots have a regular tetrahedron-shape, and quantum dots with dimension down to sub-30 nm were achieved. This is a crucial step towards future large scale production of room temperature operable SETs as device design candidate for beyond CMOS applications.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

As the geometrical scaling of silicon (Si)-based transistor approaches its physical limitations after about five decades of device scaling, high-mobility III-V semiconductors are currently under intensive research as possible candidates to replace Si as the channel material to sustain the continuous device scaling beyond 7 nm technology node. However, several critical challenges have to be overcome before III-V technology can become viable.

The objective of this thesis is to address some of the most challenging issues related to integration of III-V metal-oxide-semiconductor field-effect-transistors (MOSFETs) on Si substrate. Various novel nanoscale III-V MOSFETs device architectures and cost-effective integration process techniques have been proposed and experimentally realized in this thesis. The contributions of this thesis are listed in the next Section.

6.2 Contributions of This Thesis

6.2.1 Sub-7 nm Channel Length Junctionless Field-Effect-Transistors (JLFETs) with Band-Engineered InP/$In_{0.53}Ga_{0.47}As$/InP Channel for Improved Density-of-States (DOS)

An approach to improve DOS of InP/$In_{0.53}Ga_{0.47}As$/InP channel heterostructure by engineering the sub-band energy separation in the Γ-valley (ΔE_Γ) was presented **[185]**. Subsequently, JLFETs featuring the InP/$In_{0.53}Ga_{0.47}As$/InP channel heterostructure with $In_{0.53}Ga_{0.47}As$ thickness (T_{InGaAs}) of 1 nm and channel length (L_{CH}) down to sub-10 nm were realized. The JLFET with the shortest L_{CH} of 6 nm was demonstrated to be highly ballistic with saturation ballistic ratio (B_{SAT}) of 0.75. The extracted injection velocity (v_{x0}) surpasses that of strained Si n-channel field-effect-transistors (nFETs) by 30% in sub-10 nm L_{CH} regime.

6.2.2 Growth Optimization and Physical Modeling of $In_xGa_{1-x}As$ Growth on Ge Fins with Different Orientations

A physical modeling of the growth of GaAs on Ge fins was proposed and experimentally verified [186], [187]. Our physical model was able to explain the shapes of GaAs crystals grown on the Ge fins having different in-plane orientations. Furthermore, high-quality and selective growth of $In_{0.2}Ga_{0.8}As$ on Ge fin was achieved at a growth temperature of 640 °C and a filling factor of 95 %. Our results could pave way towards realization of high mobility III-V/Ge FinFET complementary-metal-oxide-semiconductor (CMOS) on Si platform.

6.2.3 Vertically Stacked III-V Nanowire CMOS on Si Featuring Extremely-Thin (sub-150 nm) Buffer Layer Technology

Novel vertically stacked structure comprising of InAs nanowires and GaSb nanowires on Si substrate were demonstrated. The InAs nFETs and GaSb p-channel field-effect-transistors (pFETs) were integrated on a common Si platform using a cost-effective extremely-thin (sub-150 nm) buffer layer technology for the first time [188]. Decent transfer characteristics with subthreshold swing (*SS*) of 126 mV/decade and drain induced barrier lowering (*DIBL*) of 285 mV/V were achieved for the InAs nFET with a L_{CH} of 20 nm at V_D of 0.5 V. For the vertically stacked GaSb NW pFET with a L_{CH} of 500 nm, the lowest reported *SS* of 188 mV/decade and highest I_{ON}/I_{OFF} ratio of more than 10^3 were achieved for GaSb pFETs on the Si substrate. Furthermore, a model was proposed to explain the impact of density of interface traps (D_{it}) on the electrical characteristics of InAs nFETs with different nanowire width (W_{NW}) and was verified through simulation and experimental results.

6.2.4 Novel Short-Channel Nanowire FET with Tapered Source/Drain (S/D) Structure and Quantum Dots with Self-Aligned S/D Structure

Novel short-channel junctionless nanowire field-effect-transistors (JL-NWFETs) with tapered S/D structure and quantum dot with self-aligned S/D structure were realized for the first time by exploiting anisotropic wet etch profile of III-V materials [188]. JL-NWFET devices with sub-20 nm L_{CH} and sub-20 nm W_{NW} were realized in this work. The JL-NWFET with L_{CH} of 20 nm shows good transfer characteristics with *SS* of 190 mV/decade at V_D of 0.5 V despite having a large equivalent oxide thickness (EOT) of 6 nm and high substrate doping (N_D) of 5×10^{19} cm^{-3}. Furthermore, a process to fabricate quantum dot with self-aligned S/D structure was also demonstrated. The process could pave way towards future large scale production of room temperature operable single-electron-transistor (SET).

6.3 Future Directions

6.3.1 Improving Band-Engineered III-V Channel Heterostructure

In Chapter 2, we have demonstrated that the DOS of $In_{0.53}Ga_{0.47}As$ could be improved by engineering the ΔE_Γ using InP/$In_{0.53}Ga_{0.47}As$/InP channel heterostructure. Therefore, there is a motivation to investigate other III-V channel heterostructures, as shown in Fig. 6.1(a). Furthermore, it is also interesting to explore different channel designs such as the "staircase-like" and retrograde conduction band profile, as shown in Fig. 6.1(b). These designs could increase the number of subbands near the conduction band for improved DOS.

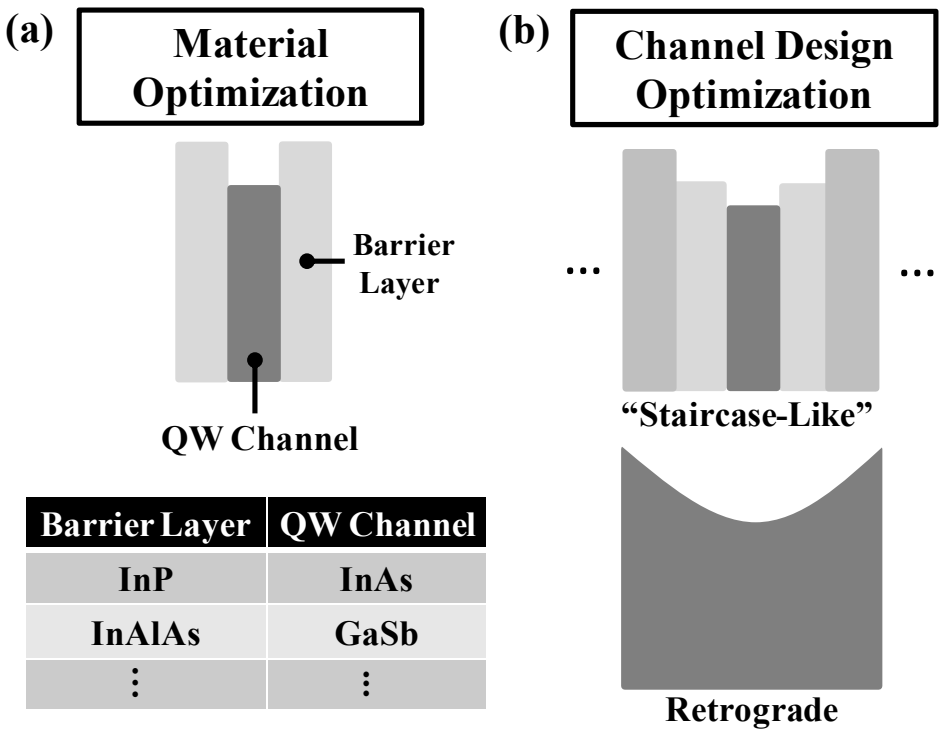


Fig. 6.1 Schematics illustrating possible ways to improve DOS of the band-engineered channel heterostructure, including using (a) different materials, and (b) using channel design with "staircase-like" or retrograde conduction band profile.

6.3.2 Further Improvements on Vertically-Stacked Nanowire CMOS Structure

(i) Channel Material Selection and Optimization of the S/D Design

In Chapter 4, we had demonstrated a promising integration approach for III-V CMOS on Si platform employing an extremely thin (sub-150 nm) buffer layer technology. The transistor performance could be further improved by using self-aligned S/D scheme or recessing the S/D so that the metal contact can form Ohmic contact to all the channel layers as shown in Fig. 6.2 (a). Furthermore, different channel material combinations such as GeSn with $In_{0.53}Ga_{0.47}As$ or InGaSb with InAs can be considered to improve the performance of pFETs and nFETs, respectively, as shown in Fig. 6.2 (b).

(ii) Vertically Stacked III-V NW CMOS with Tapered S/D Architecture

In Chapter 5, we had demonstrated a novel tapered S/D nanowire design for effective reduction in S/D series resistance. It is favorable to realize a vertically stacked nanowire CMOS structure similar to the one in Chapter 4 using the tapered S/D design for improved device

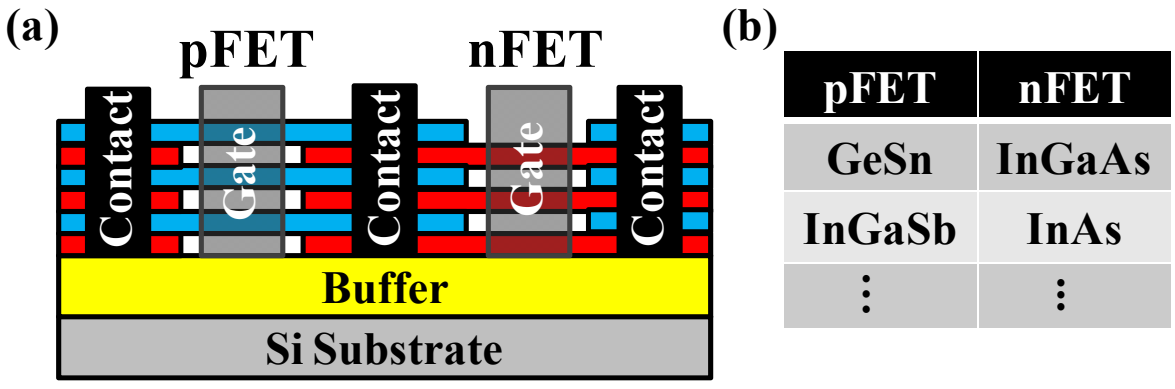


Fig. 6.2 (a) Cross-sectional schematic of a vertically stacked nanowire CMOS on Si. The S/D is recessed so that metal pad can form Ohmic contact to all channel layers. (b) Channel material candidates of pFETs and nFETs for realizing high performance vertically stacked nanowire CMOS on Si.

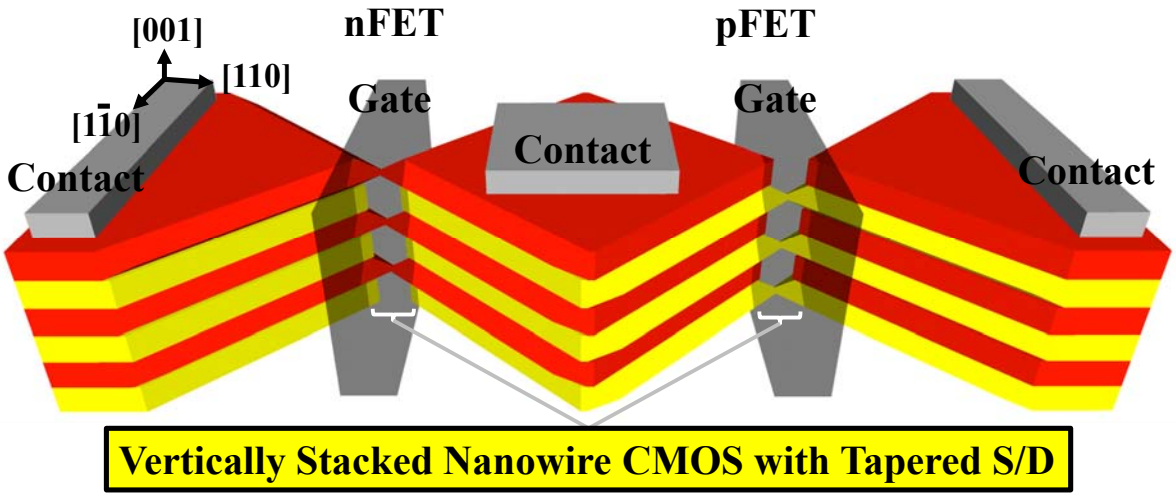


Fig. 6.3 Schematic of a vertically stacked nanowire CMOS with tapered S/D structure.

performance, as shown in Fig. 6.3. This could be achieved by exploiting the anisotropic wet etch profile of semiconductor materials. As discussed in Section 2 of Chapter 5, anisotropic wet etch profile for III-V (001) substrate along the $[\bar{1}10]$ orientation using a rectangular-shaped etch mask opening would result in etch profile with outward facing normal (OF), as shown in Fig. 6.4 (a). Thus by employing a triangular-shaped etch mask followed by anisotropic wet etching process, a nanowire with tapered S/D structure can be obtained, as shown in Fig. 6.4 (b). It is interesting to note that this approach is also applicable to Si (001) or Ge (001) substrates since they exhibit the OF anisotropic etch profile along [110] and $[\bar{1}10]$ orientations.

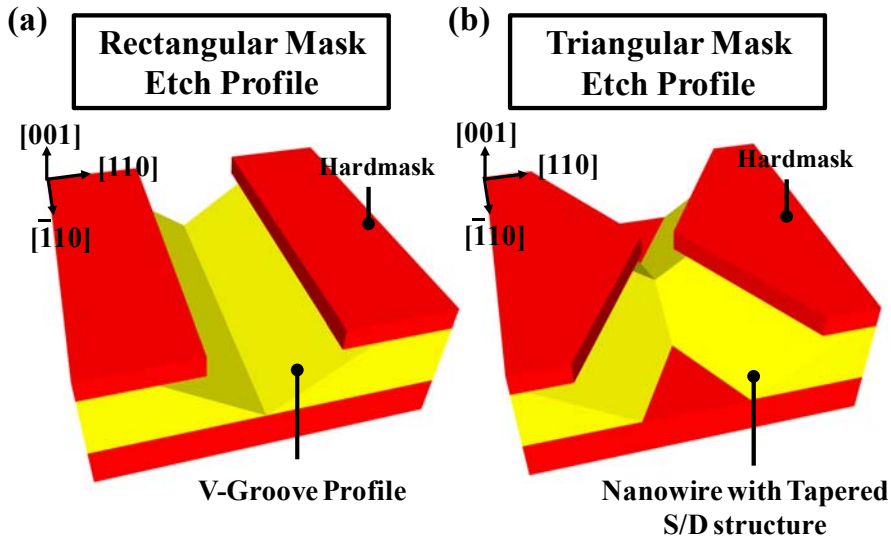


Fig. 6.4 Lateral undercut profile of Si, Ge, and III-V semiconductor materials along $[\bar{1}10]$ for (a) rectangular etch mask opening which results in a V-groove etch profile, and (b) triangular etch mask opening which results in a nanowire with tapered S/D structure.

In Fig. 6.5, a process flow to fabricate the vertically stacked nanowire CMOS with tapered S/D structure is proposed. The starting substrate should comprise of thick (more than 50 nm-thick) alternating p- and n-channel materials. First, mesa mask with hourglass-shaped is patterned on the substrate as shown by the top right schematic in Fig. 6.5. This is followed by anisotropic dry etching for mesa formation. It is important to ensure that the mesa sidewall is vertical in order to achieve a uniform nanowires cross-section in the subsequent step. Next, the hardmask is selectively removed using time controlled wet etching process. This is to ensure that a triangular mask pattern can be formed at each vertical spacing of the channel layers. Note that the nFET channel material serves as the hardmask for the pFET nanowire formation, and vice versa. After that, anisotropic wet etch process is performed to obtain the vertically stacked nanowire with tapered S/D structure. Finally, the high-*k*, metal gate, and contact formation steps, as described in Section 3 of Chapter 4, are performed to complete the device fabrication.

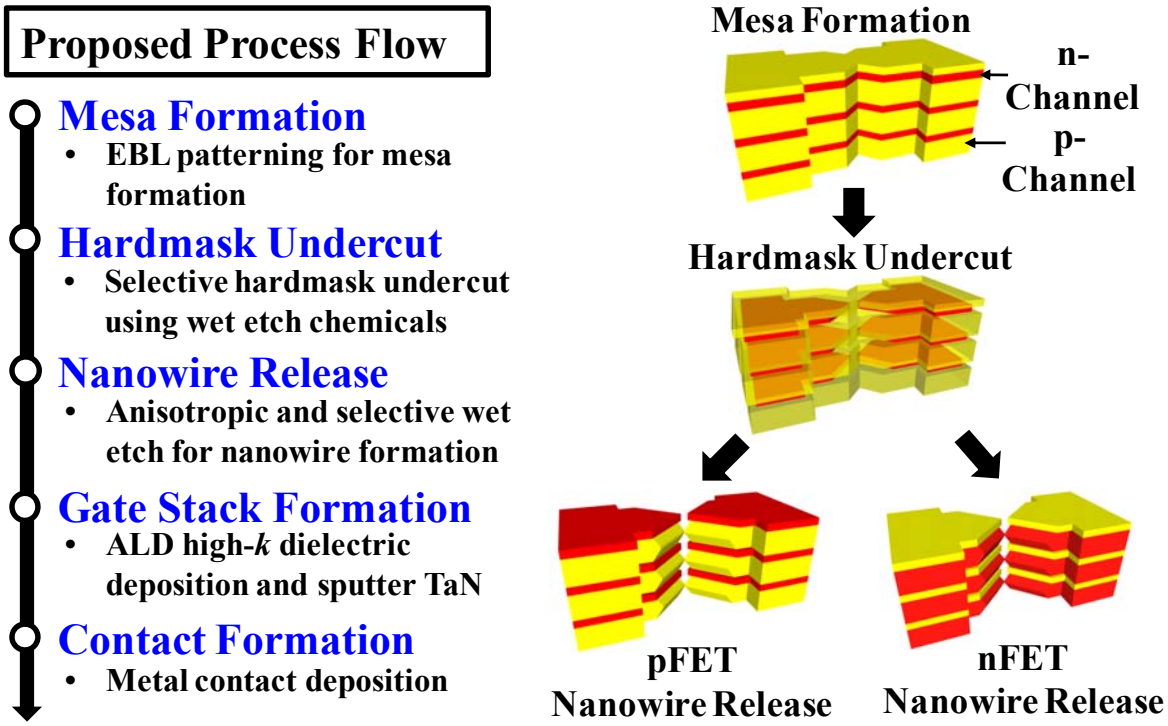


Fig. 6.5 Proposed process flow for fabricating vertically stacked nanowire CMOS with tapered S/D structure.

6.3.3 Towards Realization of Source-Filter FET Devices

Besides the tapered S/D architecture, the anisotropic wet etch profile could also be explored for single [Fig. 6.6 (a)] and multiple quantum dots structure [Fig. 6.6 (b)] by using diamond-shaped hardmask. Successful demonstration of the multiple quantum dots shown in Fig 6.6 (b) could pave way towards the realization of filter-source FET structure for achieving sub-60 mV/decade substhreshold swing.

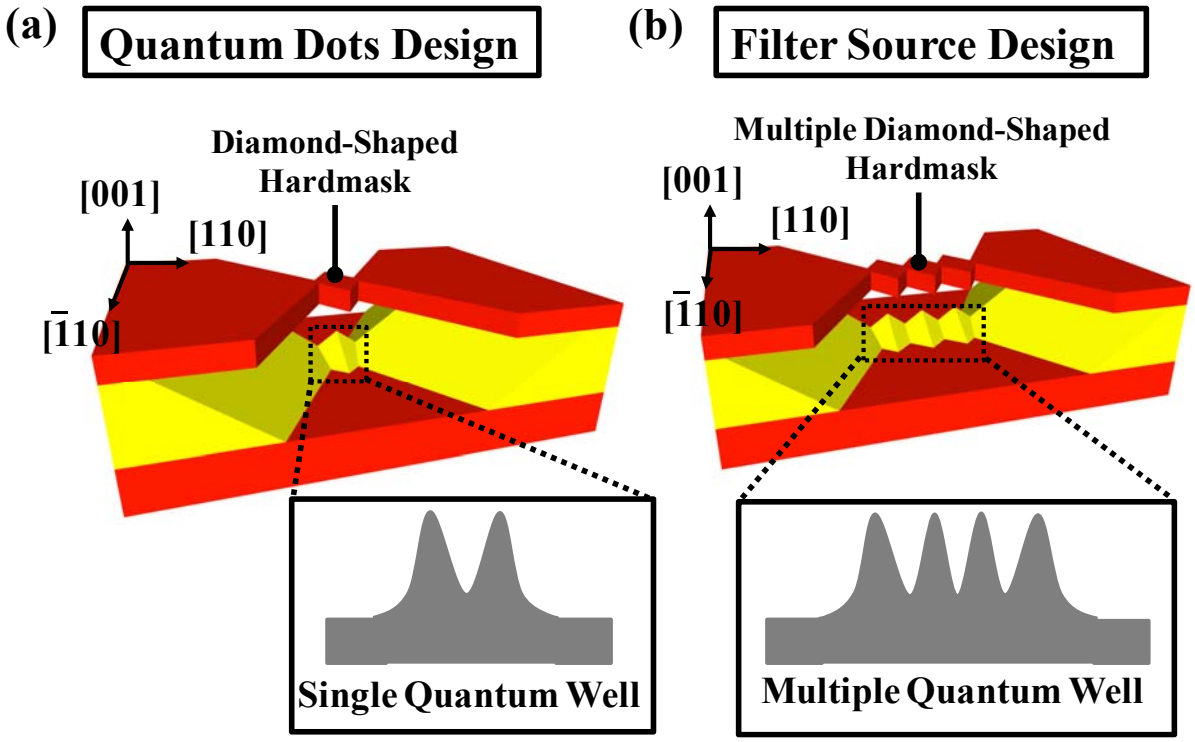


Fig. 6.6 Schematics of (a) quantum dot design and (b) filter source design realized by anisotropic wet etch process through a diamond-shaped and multiple-diamond shaped hardmask, respectively.

References

[1] G. E. Moore, "Progress in digital integrated electronics," *Technical Digest – International Electron Devices Meeting*, 1975, pp. 11-13.

[2] R. H. Dennard, F. H. Gaensslen, H. –N. Yu, V. L. Rideout, E. Bassous, and A. R. Leblanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *Journal of Solid State Circuits*, vol. **9**, no. 5, pp. 256-268, 1974.

[3] M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, "Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor field-effect transistors," *Journal of Applied Physics*, vol. **97**, no. 1, pp. 1101-1128, 2005.

[4] S. Takagi, J. L. Hoyt, J. J. Welser, and J. F. Gibbons, " Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal-oxide-semiconductor field-effect transistors," *Journal of Applied Physics*, vol. **80**, no. 3, pp. 1567-1577, 1996.

[5] T. Tezuka, N. Sugiyama, and S. Takagi, "Fabrication of strained Si on an ultrathin SiGe-on-insulator virtual substrate with a high-Ge fraction," *Applied Physics Letters*, vol. **79**, no. 12, pp. 1798-1800, 2001.

[6] Y. Sun, S. E. Thompson, and T. Nishida, "Physics of strain effects in semiconductors and metal-oxide-semiconductor firld-effect transistors," *Journal of Applied Physics*, vol. **101**, no. 10, pp. 4503-4525, 2007.

[7] C. W. Leitz, M. T. Currie, M. L. Lee, Z. –Y. Cheng, D. A. Antoniadis, and E. A. Fitzgerald, "Hole mobility enhancements and alloy scattering-limited mobility in tensile strained Si/SiGe surface channel metal-oxide-semiconductor field-effect transistors," *Journal of Applied Physics*, vol. **92**, no. 7, pp. 3745-3751, 2002.

[8] J. Robertson, "High dielectric constant gate oxides for metal oxide Si transistors," *Reports on Progress in Physics*, vol. **69**, no. 2, pp. 327-396, 2006.

[9] J. Robertson, "High dielectric constant oxides," *Europe Physics Journal of Applied Physics*, vol. **28**, no. 3, pp. 265-291, 2004.

[10] H. –S. P. Wong, "Beyond the conventional transistors," *IBM Journal of Research and Development*, vol. **46**, no. 2.3, pp. 133-168, 2002.

[11] D. Hisamoto, W. –C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T, -J. King, J. Bokor, and C. Hu, "FinFET – a self aligned double-gate MOSFET scalable to 20 nm," *IEEE Transactions on Electron Devices*, vol. **47**, no. 12, pp. 2320-2325, 2000.

[12] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Ho, Q. Xiang, T. –J. King, J. Bokor, C. Hu, M. –R. Lin, and D. Kyser, " FinFET scaling to 10 nm gate length," *Technical Digest – International Electron Devices Meeting*, 2002, pp. 251-254.

[13] M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, " HfO_2 and Al_2O_3 gate dielectrics on GaAs grown by atomic layer deposition," *Applied Physics Letters*, vol. **86**, no. 15, pp. 2904-2907, 2005.

[14] Y. Xuan, Y. Q. Wu, and P. D. Ye, "High-performance inversion-type enhancement-mode InGaAs MOSFET with maximum drain current exceeding 1A/mm," *IEEE Electron Device Letters*, vol. **29**, no. 4, pp. 294-296, 2008.

[15] S. Takagi, T. Irisawa, T. Tezuka, T. Numata, S. Nakaharai, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake, M. Shichijo, R. Nakane, S. Sugahara, M. Yakenaka, and N. Sugiyama, "Carrier-transport-enhanced channel CMOS for improved power consumption and performance," *IEEE Transactions on Electron Devices*, vol. **55**, no. 1, pp. 21-39, 2008.

[16] P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H. –J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent. M. Hong. K. K. Ng, and J. Bude, "GaAs MOSFET with oxide gate dielectric grown by atomic layer deposition," *IEEE Electron Device Letters*, vol. **24**, no. 4, pp. 209-211, 2003.

[17] R. J. W. Hill, D. A. J. Moran, X. Li, H. Zhou, D. Macintyre, S. Thoms. A. Asenov, P. Zurcher, K. Rajagopalan, J. Abrokwah, R. Droopad, M. Passlack, and I. G. Thayne, "Enhancement-mode GaAs MOSFETs with an $In_{0.3}Ga_{0.7}As$ Channel, a mobility over 5000 $cm^2/V.s$, and transconductance of over 475 μS/μm," *IEEE Electron Device Letters*, vol. **28**, no. 12, pp. 1080-1082, 2007.

[18] S. Oktyabrsky, and P. D. Ye, "Fundamentals of III-V semiconductor MOSFETs," *Springer*, New York, 2009.

[19] S. Takagi, "Re-examination of subband structure engineering in ultra-short-channel MOSFETs under ballistic carrier transport," *Technology Digest – Symposium of VLSI*, 2003, pp. 115-116.

[20] D. Zubia, S. Zhang, R. Bommena, X. Sun, S. R. J. Brueck, and S. D. Hersee, "Initial growth stages of nanoheteroepitaxial GaAs on Si(100) by OMVPE," *Journal of Electronic Materials*, vol. **30**, pp. 812-816, 2001.

[21] R. M. Sieg, J. A. Carlin, J. J. Boeckl, S. A. Ringel, M. T. Currie, S. M. Ting, T. A. Langdo, G. Taraschi, E. A. Fitzgerald, and B. M. Keyes, "High minority-carrier lifetimes in GaAs grown on low-defect-density Ge/GeSi/Si substrates," *Applied Physics Letters*, vol. **73**, no. 21, pp. 3111-3113, 1998.

[22] G. Vanamu, A. K. Datyel, and S. H. Zaidi, " Epitaxial growth of high-quality Ge films on nanostructured silicon substrates," *Applied Physics Letters*, vol. **88**, no. 20, pp. 1909-1912, 2006.

[23] J. Z. Li, J. Bai, J. –S. Park, B. Adekore, K. Fo, M. Caroll, A. Lochtefeld, and Z. Shellenbarger, "Defect reduction of GaAs/Si epitaxy by aspect ratio trapping," *Applied Physics Letters*, vol. **91**, no. 2, pp. 1114-1117, 2007.

[24] N. Waldron, C. Merckling, L. Teugels, P. Ong, S. A. U. Ibrahim, F. Sebaai, A. Pourghaderi, K. Barla, N. Collaert, and A. V. –Y. Thean, "InGaAs gate-all-around nanowire devices on 300 mm Si substrates," *IEEE Electron Device Letters*, vol. **35**, no. 11, pp. 1097-1099, 2014.

[25] K. Hjort, "Transfer of InP epilayers by wafer bonding," *Journal of Crystal Growth*, vol. **268**, no. 3, pp. 346-358, 2004.

[26] S. –H. Kim, M. Yokoyama, N. Taoka, R. Iida, S. Lee, R. Nakane, Y. Urabe, N. Miyata, T. Yasuda, H. Yamada, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi, "High performance extremely-thin body III-V-on-insulator MOSFETs on a Si substrate with Ni-InGaAs metal S/D and MOS interface buffer engineering," *Technical Digest – Symposium of VLSI*, 2011, pp. 58-59.

[27] K. Takei, M. Madsen, H. Fang, R. Kapadia, S. Chuang, H. –S. Kim, C. –H. Liu, E. Plis, J. Nah, S. Krishna, Y. –L. Chueh, J. Guo, and A. Javey, "Nanoscale InGaSb heterostructure membranes on Si substrates for high hole mobility transistors," *Nano Letters*, vol. **12**, no. 4, pp. 2060-2066, 2012.

[28] J. Nah, H. Fang, C. Wang, K. Takei, M. –H. Lee, E. Plis, S. Krishna, and A. Javey, "III-V complementary metal-oxide-semiconductor electronics on silicon substrates," *Nano Letters*, vol. **12**, no. 7, pp. 3592-3595, 2012.

[29] L. Czornomaz, N. Daix, K. Cheng, D. Caimi, C. Rossel, K. Lister, M. Souza, and J. Fompeyrine, "Co-integration of InGaAs n- and SiGe p-MOSFETs into digital CMOS circuits using hybrid dual-channel ETXOI substrates," *Technical Digest – International Electron Devices Meeting,* 2013, pp. 53-55.

[30] M. Yokoyama, H. Yokoyama, M. Takenaka, and S. Takagi, "III-V single structure CMOS by using ultrathin body InAs/GaSb-OI channels on Si," *Technical Digest – Symposium of VLSI*, 2014, pp. 1-2.

[31] M. J. H. van Dal, G. Vellianitis, B, Duriez, G. Doornbos, C. –H. Hsieh, B. –H. Lee, K. –M. Yin, M. Passlack, and C. H. Diaz, "Germanium p-channel FinFET fabricated by aspect ratio trapping," *IEEE Transaction on Electron Devices*, vol. **61**, no. 2, pp. 430-436, 2014.

[32] Y. Liang, W. D. Nix, P. B. Griffin, and J. D. Plummer, "Critical thickness enhancement of epitaxial SiGe films grown on small structure," *Journal of Applied Physics*, vol. **97**, no. 4, pp. 3519-3526, 2005.

[33] H. –C. Chin, X. Gong, T. K. Ng, W. K. Loke, C. P. Wong, Z. Shen, S. Wicaksono, S. F. Yoon, and Y. –C. Yeo, "Nanoheteroepitaxy of gallium arsenide on strain-compliant silicon-germanium nanowires," *Journal of Applied Physics*, vol. **108**, no. 2, pp. 4312-4317, 2010.

[34] D. Zubia, and S. D. Hersee, "Nanoheteroepitaxy: The application of nanostructuring and substrate compliance to the heteroepitaxy of mismatched semiconductor materials," *Journal of Applied Physics*, vol. **85**, no. 9, pp. 6492-6496, 1999.

[35] J. –T. Park, and J. –P. Collinge, "Multiple-gate SOI MOSFETs: Device design guidelines," *IEEE Transactions on Electron Devices*, vol. **49**, no. 12, pp. 2222-2229, 2002.

[36] D. G. -Gordon, H. Shtrikman, D. Mahalu, D. A. -Magder, U. Meirav, and M. A. Kastner, "Kondo effect in a single-electron transistor," *Nature*, vol. **391**, no. 6663, pp. 156-159, 1998.

[37] J. Park, A. N. Pasupathy, J. I. Goldsmith, C. Chang, Y. Yaish, J. R. Petta, M. Rinkoski, J. P. Sethna, H. D. Abruna, P. L. McEuen, an D. C. Ralph, "Coulomb blockade and the Kondo effect in single-atom transistor," *Nature*, vol. **417**, no. 6890, pp. 722-725, 2002.

[38] R. H. Mathews, J. P. Sage, T. C. L. G. Sollner, S. D. Calawa, C. –L Chen, L. J. Mahoney, P. A. Maki, and K. M. Molvar, "A new RTD-FET logic family," *Proceeding of IEEE*, vol. **87**, no. 4, pp. 596-605, 1999.

[39] H. Hasegawa and H. Ohno, "Unified disorder induced gap state model for insulator-semiconductor and metal-semiconductor interfaces," *Journal of Vacuum Science Technology B*, vol. **4**, no. 4, pp. 1130-1138,1986.

[40] M. Hong, J. R. Kwo, P. –C. Tsai, Y. Chang, M. –L. Huang, C. –P. Chen, and T. –D. Lin, "III-V metal-oxide-semiconductor field-effect transistor with high-*k* dielectric," *Japan Journal of Applied Physics*, vol. **46**, no. 5B, pp. 3167-3180, 2007.

[41] P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, S. N. G. Chu, S. Nakahara, H.-J. L. Grossmann, J. P. Mannaerts, M. Hong, K. K. Ng, and J. Bude, "GaAs metal-oxide-semiconductor

field-effect transistor with nanometer-thin dielectric grown by atomic layer deposition," *Applied Physics Letters*, vol. **83**, no. 1, pp. 180-182, 2003.

[42] M. L. Huang, Y. C. Chang, C. H. Chang, Y. J. Lee, P. Chang, J. Kwo, T. B. Wu, and M. Hong, "Surface passivation of III-V compound semiconductors using atomic-layer-deposition-grown Al_2O_3," *Applied Physics Letters*, vol. **87**, no. 25, pp. 2104-2106, 2005.

[43] M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, "HfO_2 and Al_2O_3 gate dielectrics on GaAs grown by atomic layer deposition," *Applied Physics Letters*, vol. **86**, no. 15, pp. 2904-2906, 2005.

[44] C. –H. Chang, Y. –K. Chiou, Y. –C. Chang, K. –Y. Lee, T. D. Lin, T. B. Wu, M. Hong, and J. Kwo, "Interfacial self-cleaning in atomic layer deposition of HfO_2 gate dielectric on $In_{0.15}Ga_{0.85}As$,"*Applied Physics Letters*, vol. **89**, no. 24, pp. 2911-2913, 2006.

[45] A. Alian, G. Brammertz, W. Waldron, C. Merckling, G. Hellings, H. C. Lin, W. E. Wang, M. Meuris, E. Simoenm, K. De Meyer, and M. Heyns, "Silicon and Selenium implantation and activation in $In_{0.53}Ga_{0.47}As$ under low thermal budget conditions," *Microelectronic Engineering,* vol. **88**, no. 2, pp. 155-158, 2011.

[46] X. Zhang, H. Guo, X. Gong, Q. Zhou, Y.-R. Lin, H.-Y. Lin, C.-H. Ko, C. H. Wann, and Y.-C. Yeo, "$In_{0.7}Ga_{0.3}As$ channel n-MOSFET with self-aligned Ni-InGaAs source and drain," *Electrochemical Solid-State Letters*, vol. **14**, no. 2, pp. 60-62, 2011.

[47] X. Zhang, H. Guo, H.-Y. Lin, Ivana, X. Gong, Q. Zhou, Y.-R. Lin, C.-H. Ko, C. H. Wann, and Y.-C. Yeo, "Reduction of off-state leakage current in $In_{0.7}Ga_{0.3}As$ channel n-MOSFETs with self-aligned Ni-InGaAs contact metallization," *Electrochemical Solid-State Letters*, vol. **14**, no. 5, pp. 212-214, 2011.

[48] X. Zhang, H. Guo, X. Gong, Q. Zhou, H.-Y. Lin, Y.-R. Lin, C.-H. Ko, C. H. Wann, and Y.-C. Yeo, "$In_{0.7}Ga_{0.3}As$ channel n-MOSFETs with a novel self-aligned Ni-InGaAs contact formed using a salicide-like metallization process," in *Proceedings of the VLSI Technology, Systems and Application* (*VLSI-TSA)*, *IEEE*, 2011, pp. 26-27.

[49] Ivana, J. Pan, Z. Zhang, X. Zhang, H. Guo, X. Gong, and Y.-C. Yeo, "Photoelectron spectroscopy study of band alignment at interface between Ni-InGaAs and $In_{0.53}Ga_{0.47}As$," *Applied Physics Letters*, vol. **99**, no. 1, pp. 2105-2107, 2011.

[50] X. Zhang, Ivana, H. Guo, X. Gong, Q. Zhou, and Y.-C. Yeo, "A self-aligned Ni-InGaAs contact technology for InGaAs channel n-MOSFETs," *Journal of the Electrochemical Society*, vol. **159**, no. 5, pp. 511-520, 2012.

[51] J. A. del Alamo, "Nanometre-scale electronics with III–V compound semiconductors," *Nature*, vol. **479**, no. 7373, pp. 317-323, 2011.

[52] A. Rahman, G. Klimeck, and M. Lundstrom, "Novel channel materials for ballistic nanoscale MOSFETs–bandstructure effects," *Technical Digest – International Electron Devices Meeting*, 2005, pp. 604–607.

[53] R. Kim, T. Rakshit, R. Kotlyar, S. Hasan, and C. E. Weber, "Effects of surface orientation on the performance of idealized III–V thin-body ballistic n-MOSFETs," *IEEE Electron Device Lett*ers, vol. **32**, no. 6, pp. 746–748, 2011.

[54] M. Luisier, "Performance comparison of GaSb, strained-Si, and InGaAs double-gate ultrathin-body n-FETs," *IEEE Electron Device Lett*ers, vol. **32**, no. 12, pp. 746–748, 2011.

[55] K. Alam, S. Takagi, and M. Takenaka, "Analysis and comparison of L-valley transport in GaAs, GaSb, and Ge ultrathin-body ballistic nMOSFETs," *IEEE Transactions on*

Electron Devices, vol. **60**, no. 12, pp. 4213–4218, 2013.

[56] K. Majumdar and N. Bhat, "Bandstructure effects in ultra-thin-body double-gate field effect transistor: A fullband analysis," *Journal of Applied Phys*ics, vol. **103**, no. 11, pp. 4503-4512, 2008.

[57] Z. Yuan, A. Nainani, X. Guan, H.-S. Wong, and K. C. Saraswat, "Tight-binding study of Γ-L bandstructure engineering for ballistic III-V nMOSFETs," *in Proceeding of International Conference on Simulation of Semiconductor Processes and Devices*, 2011, pp. 71-74.

[58] H. Fang, S. Chuang, K. Takei, H. S. Kim, E. Plis, C. H. Liu, S. Krishna, Y. L. Chueh, and A. Javey, "Ultrathin-body high-mobility InAsSb-on-insulator field-effect transistors," *IEEE Electron Device Lett*ers, vol. **33**, no. 4, pp. 504-506, 2012.

[59] A. Paul, S. Mehrotra, G. Klimeck, and M. Rodwell, "Performance enhancement of GaAs UTB pFETs by strain, orientation and body thickness engineering," *in Proceeding of Device Research Conference*, 2011, pp. 233-234.

[60] J. B. Roldan, F. Jimenez-Molinos, M. Balaguer, and F. Gamiz, "An in-depth Monte Carlo study of low-field mobility in ultra-thin body DGMOSFETs for modeling purposes," *Solid-State Electronics*, vol. **79**, pp. 92-97, 2013.

[61] K. Majumdar and N. Bhat, "Bandstructure effects in ultra-thin-body double-gate field effect transistor: A fullband analysis," *Journal of Applied Phys*ics, vol. **103**, no. 11, pp. 4503-4512, 2008.

[62] K. Takei, S. Chuang, H. Fang, R. Kapadia, C. H. Liu, J. Nah, H. S. Kim, E. Plis, S. Krishna Y. L. Chueh, and A. Javey, "Benchmarking the performance of ultrathin body InAs-on-insulator transistors as a function of body thickness," *Applied Physics Letters*,

vol. **99**, no. 10, pp. 3507-3510, 2011.

[63] H. Fang, S. Chuang, K. Takei, H. S. Kim, E. Plis, C. H. Liu, S. Krishna, Y. L. Chueh, and A. Javey, "Ultrathin-body high-mobility InAsSb-on-insulator field-effect transistors," *IEEE Electron Device Lett*ers, vol. **33**, no. 4, pp. 504-506, 2012.

[64] M. Rodwell, W. Frensley, S. Steiger, E. Chagarov, S. Lee, H. Ryu, Y. Tan, G. Hegde, L. Wang, J. Law, T. Boykin, G. Klimek, P. Asbeck, A. Kummel, and J. N. Schulman, "III-V FET channel designs for high current densities and thin inversion layers," ," *in Proceeding of Device Research Conference*, 2010, pp. 149-152.

[65] R. Kim, T. Rakshit, R. Kotlyar, S. Hasan, and C. E. Weber, "Effects of surface orientation on the performance of idealized III-V thin body ballistic n-MOSFETs," *IEEE Electron Device Letters*, vol. **32**, no. 6, pp. 746-748, 2011.

[66] Q. Rafhay, R. Clerc, M. Ferrier, G. Pananakakis, and G. Ghibaudo, "Impact of channel orientation on ballistic current of nDGFETs with alternative channel materials," *Solid-State Electron*ics, vol. **52**, no. 4, pp. 540-547, 2008.

[67] M. Luisier, "Performance comparison of GaSb, strained-Si, and InGaAs double-gate ultrathin-body n-FETs," *IEEE Electron Device Lett*ers, vol. **32**, no. 12, pp. 1686-1688, 2011.

[68] Y. Guo, X. Zhang, K. Low, K.-T. Lam, Y.-C. Yeo, and G. Liang, "Effect of body thickness on the electrical performance of ballistic n-channel GaSb double-gate ultra-thin-body transistor," *IEEE Transactions on Electron Devices*, vol. **62**, no. 3, pp. 788-794, 2015.

[69] R. M. Saumitra, M. Povoloskyi, D. C. Elias, T. Kubis, J.J. M. Law, M.J.W. Rodwell, and G. Klimeck, "Simulation study of thin–body ballistic n-MOSFETs involving transport in

mixed Γ-L valleys," *IEEE Electron Device Lett*ers, vol. **34**, no. 9, pp. 1196-1198, 2013.

[70] M. Yokoyama, H. Yokoyama, M. Takenaka, and S. Takagi, "III-V single structure CMOS by using ultrathin body InAs/GaSb-OI channels on Si," *Technology Digest – Symposium of VLSI*, 2014, pp. 34-35.

[71] M. Yokoyama, K. Nishi, S. Kim, H. Yokoyama, M. Takenaka, and S. Takagi, "Self-aligned Ni-GaSb source/drain junctions for GaSb p-channel metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters, v*ol. **104**, no. 9, pp. 3509-3512, 2014.

[72] K. Nishii, M. Yokoyama, T. Hoshi, H. Sugiyama, M. Takenaka, and S. Takagi, "Operation of the GaSb p-channel metal-oxide-semiconductor field-effect transistors fabricated on {111}A surfaces," *Applied Physics Letters,* vol. **105**, no. 23, pp. 3503-3506, 2014.

[73] R. L. Zhu, T. H. Chiang, W. J. Hsueh, K. H. Chen, K. Y. Lin, G. J. Brown, J. I. Chyi, J. Kwo, and M. Hong, "Passivation of GaSb using molecular beam epitaxy Y_2O_3 to achieve low interfacial trap density and high-performance self-aligned inversion-channel p-metal-oxide-semiconductor field-effect-transistors," *Applied Physics Letters,* vol. **105**, no. 18, pp. 2106-2111, 2014.

[74] S. E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Z. Ma, B. Mcintyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. E.–Mansy, "A logic nanotechnology featuring strained-silicon," *IEEE Electron Device Lett*ers, vol. **25**, no. 4, pp. 191-193, 2004.

[75] S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial-process-induced strained-Si: extending the CMOS roadmap," *IEEE Transactions on Electron Devices*, vol. **53**, no. 5, pp. 1010-1020, 2006.

[76] K. Brunner, "Si/Ge nanostructures," *Report on Progress in Phys*ics, vol. **65**, no. 1, pp. 27-72, 2001.

[77] S. H. Park, Y. Liu, N. Kharche, M. S. Jelodar, G. Klimeck, M. S. Lundstrom, and M. Luisier, "Performance comparisons of III-V and strained-Si on planar FETs and nonplanar FinFETs at ultrashort gate length (12 nm)," *IEEE Transactions on Electron Devices*, vol. **59**, no. 8, pp. 2107-2114, 2012.

[78] K. H. Goh, Y. Guo, X. Gong, G. Liang, and Y.-C. Yeo, "Near ballistic sub-7 nm $In_{0.53}Ga_{0.47}As$ junctionless FET featuring 1 nm extremely-thin channel and raised S/D structure," *Technical Digest – International Electron Devices Meeting*, 2013, pp. 433–436.

[79] A. Majumdar and D. A. Antoniadis, "Analysis of carrier transport in short-channel MOSFETs," *IEEE Transactions on Electron Devices*, vol. **61**, no. 2, pp. 351-358, 2014.

[80] P. Vogl, H. P. Hjalmarson, and J. D. Dow, "A semi-emperical tight-binding theory of the electronic structure of semiconductor", *Journal of Physics Chemistry Solids,* vol. 44, no. 5, pp. 365-378, 1983.

[81] J.-M. Jancu, R. Scholz, F. Beltram, and F. Bassani, "Empirical spds∗ tight-binding calculation for cubic semiconductors: General method and material parameters," *Physic. Review B, Condensed. Matter*, vol. 57, no. 11, pp. 6493–6507, 1998.

[82] M. Luisier and G. Klimeck, "Investigation of $In_xGa_{1-x}As$ ultra-thin-body tunneling FETs using a full-band and atomistic approach", *in Proceeding SISPAD*, 2009, pp. 67-70.

[83] S. Lee, F. Oyafuso, P. von Allmen, and G. Klimeck, "Boundary conditions for the electronic structure of finite-extent embedded semiconductor nanostructures," *Physics Review B*, vol. **69**, no. 4, pp. 5316-5323, 2004.

[84] A. Nishida, K. Hasegawa, R. Ohama, S. Fujikawa, S. Hara, and H. I. Fujishiro, "Comparative study on nano-scale III-V double-gate MOSFETs with various channel materials," *Physics Status Solidi C*, vol. **10**, no. 11, pp. 1413-1416, 2013.

[85] E. D. Marshall, W. X. Chen, C. S. Wu, S. S. Lau, and T. F. Kuech, "Non-alloyed ohmic contact to n-GaAs by solid-phase epitaxy," *Applied Physics Letters*, vol. **47**, pp. 298, 1985.

[86] D. A. Ahmari, M. L. Hattendorf, D. F. Lemmehirt, Q. Yang, Q. J. Hartmann, J. E. Baker, and G. E. Stillman, "Effects of alloy ambient on PdGe contacts to n-type GaAs," *Applied Physics Letters*, vol. **72**, pp. 3479, 1998.

[87] A. Khakifirooz and D. A. Antoniadis, "Transistor performance scaling: The role of virtual source velocity and its mobility dependence," *Technical Digest – International Electron Devices Meeting*, 2006, pp. 1–4.

[88] A. Khakifirooz and D. A. Antoniadis, "MOSFET performance scaling-Part 1: Historical trends," *IEEE Transactions on Electron Devices*, vol. **55**, no. 6, pp. 1391-1400, 2008.

[89] A. Khakifirooz, O. M. Nayfeh, and D. A. Antoniadis, "A simple semi-empirical short-channel MOSFET current-voltage model continuous across all regions of operation and employing only physical parameters," *IEEE Transactions on Electron Devices*, vol. **56**, no. 8, pp. 1674-1680, 2009.

[90] S. Li, Y. Hu, Y. Wu, D. Huang, P. D. Ye, and M.-F. Li, "Electronic transport in InGaAs/Al_2O_3 nFinFETs," *Semiconductor Science and Technology*, vol. **29**, no. 7, pp. 5014-5020, 2014.

[91] M. V. Fischetti and S. E. Laux, "Long-range Coulomb interactions in small Si devices. Part I: Performance and reliability," *Journal of Applied Phys*ics, vol. **89**, no. 2, pp. 1205-

1231, 2001.

[92] T. Uechi, T. Fukui, and N. Sano, "3D Monte Carlo simulation including full Coulomb interaction under high electron concentration regimes," *Physics Status Solidi C*, vol. **5**, no. 1, pp. 102-106, 2008.

[93] A. Khakifirooz and D. Antoniadis, "Transistor performance scaling: the role of virtual source velocity and its mobility dependence," *Technical Digest – International Electron Devices Meeting*, 2008, pp. 667-671.

[94] G. Brammertz, M. Caymax, M. Meuris, M. Heyns, Y. Mols, S. Degroote, and M. Leys, "GaAs on Ge for CMOS," *Thin Solid Films*, vol. **517**, no. 1, pp. 148-151, 2008.

[95] S. Takagi, T. Tezuka, T. Irisawa, S. Nakaharai, T. Numata, K. Usuda, N. Suiyama, M. Shichijo, R. Nakane, and S. Sugahara, "Device structures and carrier transport properties of advanced CMOS using high mobility channels," *Solid State Electronics*, vol. **51**, no. 4, pp. 526-536, 2007.

[96] S. Takagi, T. Irisawa, T. Tezuka, T. Numata, S. Nakaharai, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake, M. Shichijo, R. Nakane, S. Sugahara, M. Takenaka, and N. Sugiyama, "Carrier-transport-enhanced channel CMOS for improved power consumption and performance," *IEEE Transactions on Electron Devices*, vol. **55**, no. 1, pp. 21-39, 2008.

[97] D. Zubia, S. Zhang, R. Bommena, X. Sun, S. R. J. Brueeck, and S. D. Hersee, "Initial nanoheteroepitaxial growth stages of GaAs on Si(100) by OMVPE," *Journal of Electronic Materials*, vol. **30**, no. 7, pp. 812-816, 2001.

[98] K. Hjort, "Transfer of InP epilayers by wafer bonding," *Journal of Crystal Growth*, vol. **268**, no. 3, pp. 346-358, 2004.

[99] P. Chen, Y. Jing, S. S. Lau, D. Xu, L. Mawst, T. L. Alford, C. Paulson, and T. F. Kuech, "Effects of hydrogen implantation temperature on InP surface blistering," *Applied Physics Letters*, vol. **92**, no. 20, pp. 2107-2110, 2008.

[100] R. M. Sieg, J. A. Carlin, J. J. Boeckl, S. A. Ringel, M. T. Currie, S. M. Ting, T. A. Langdo, G. Taraschi, E. A. Fitzgerald, and B. M. Keyes, "High minority-carrier lifetimes in GaAs grown on low-defect-density Ge/GeSi/Si substrates," *Applied Physics Letters*, vol. **73**, no. 21, pp. 3111-3113, 1998.

[101] G. Vanamu, A. K. Datye, R. Dawson, and S. H. Zaidi, "Epitaxial growth of high-quality Ge films on nanostructured silicon substrates," *Applied Physics Letters*, vol. **88**, no. 25, pp. 1909-1912, 2006.

[102] J. Z. Li, J. Bai, J. -S. Park, B. Adekore, K. Fox, M. Caroll, A. Lochtefeld, and Z. Shellenbarger, "Defect reduction of GaAs epitaxy on Si (001) using selective aspect ratio trapping," *Applied Physics Letters*, vol. **91**, no. 2, pp. 1114-1117, 2007.

[103] Y. Liang, W. D. Nix, P. B. Griffin, and J. D. Plummer, "Critical thickness enhancement of epitaxial SiGe films grown on small structures," *Journal of Applied Physics*, vol. **97**, no. 4, pp. 3519-3529, 2005.

[104] H.-C. Chin, X. Gong, T. K. Ng, W. K. Loke, C. P. Wong, Z. Shen, S. Wicaksono, S. F. Yoon, and Y.-C. Yeo, "Nanoheteroepitaxy of gallium arsenide on strain-compliant silicon-germanium nanowires," *Journal of Applied Physics*, vol. **108**, no. 2, pp. 4312-4322, 2010.

[105] K. Mizuguchi, N. Hayafuji, S. Ochi, T. Murotani, and K. Fujikawa, "MOCVD GaAs growth on Ge (100) and Si (100) substrates," *Journal of Crystal Growth*, vol. **77**, no. 1, pp. 509-514, 1986.

[106] P. R. Pukite and P. I. Cohen, "Suppression of antiphase domains in the growth of GaAs on Ge (100) by molecular beam epitaxy," *Journal of Crystal Growth*, vol. **81**, no. 1, pp. 214-220, 1987.

[107] K. H. Goh, Y. Cheng, K. L. Low, E. Y. J. Kong, C.-K. Chia, E.-H. Toh, and Y.-C. Yeo, "Physical model for gallium arsenide growth on germanium fins with different orientations formed on 10° offcut germanium-on-insulator substrate," *Journal of Applied Physics*, vol. **113**, no. 4, pp. 4103-4113, 2013.

[108] N. Miyata, H. Ishii, Y. Urabe. T. Itatani, T. Yasuda. H. Yamada, N. Fukuhara, M. Hata, M. Deura, M. Sugiyama, M. Takenaka, and S. Takagi, "Origin of electron mobility enhancement in (111)-oriented InGaAs channel metal-insulator-semiconductor field-effect-transistors," *Microelectronic Engineering*, vol. **88**, no. 12, pp. 3459-3461, 2011.

[109] H. Ishii, N. Miyata, Y. Urabe, T. Itatani, T. Yasuda, H. Yamada, N. Fukuhara, M. Hata, M. Deura, M. Sugiyama, M. Takenaka, and S. Takagi, "High electron mobility metal-insulator-semiconductor field-effect-transistors fabricated on (111)-oriented InGaAs channels," *Applied Physics Express*, vol. **2**, no. 12, pp. 1101-1104, 2009.

[110] R. Tyagi, M. Singh, M. Thirumavalavan, T. Srinavasan, and S. K. Agarwal, "The influence of As and Ga prelayers on the metal-organic chemical vapor deposition of GaAs/Ge," *Journal of Electronic Materials*, vol. **31**, no. 3, pp. 234-237, 2002.

[111] J.-H. Lee, H. Suzuki, X. Han, M. Inagaki, K. Ikeda, N. Kojima, Y. Oshita, and M. Yamaguchi, "Low temperature growth GaAs on Ge by chemical beam epitaxy," *35th IEEE Photovoltaic Specialists Conference*, 2010, pp. 2070-2073.

[112] G. Wulff, "Zeitschrift für Kristallographie," *Crystalline Materials*, vol. **34**, no. 1, pp. 449-530, 1901.

[113] D. P. Peng, S. J Osher, B. Merriman, and H. K. Zhao, "The geometry of Wulff crystal shapes and its relations with Riemann problems," *Contemporary Mathematics*, vol. **238**, no. 6, pp. 251-303, 1999.

[114] P. S. Wong, B. L. Liang, J. Tatebayashi, L. Xue, N. Nuntawong, M. N. Kutty, S. R. J. Brueck, and D. L Huffaker, "Fabrication and characteristics of broad-area light-emitting diode based on nanopatterned quantum dots," *Nanotechnology*, vol. **20**, no. 3, pp. 5302-5312, 2009.

[115] S. W. Ping, B. Liang, R. Molecke, J. Tatebayashi, and D. L. Huffaker, "Controlled formation and Wulff simulation of equilibrium crystal shapes of GaAs pyramidal structures on nano-patterned substrates," *Crystal Growth and Design*, vol. **10**, no. 6, pp. 2509-2514, 2010.

[116] R. J. Jaccodine, "Surface energies of Germanium and Silicon", *Journal of The Electrochemical Society*, vol. 101, no. 6, pp. 524-527, 1963.

[117] N. Moll, A. Kley, E. Pehlke, and M. Scheffler, "GaAs equilibrium crystal shape from first principles", *Physical Review B*, vol. 54, no. 12, pp. 8844-8855, 1996.

[118] J. Platen, A. Kley, C. Setzer, K. Jacobi, P. Ruggerone, and M. Scheffler, "The importance of high-index surfaces for the morphology of GaAs quantum dots", *Journal of Apllied Physics*, col. 85, no. 7, pp. 3597-3601, 1999.

[119] D. K. Biegelson, R. D. Bringans, J. E. Northrup, and L.-E. Swartz, "Reconstrution of GaAs (111)B surfaces observed by scanning tunneling microscopy", *Physical Review Letter*, vol. 65, no. 452, 1990.

[120] J. Bai, J.-S. Park, Z. Cheng, M. Curtin, and B. Adekore, "Study of the defect elimination mechanisms in aspect ratio trapping Ge Growth," *Applied Physics Letters*, vol. **90**, no. 10, pp. 1902-1905, 2007.

[121] H. Klapper, "Generation and propagation of dislocations during crystal growth", *Materials Chemistry and Physics*, vol. 66, pp. 101-109, 2000.

[122] M. Yokoyama, H. Yokoyama, M. Takenaka, and S. Takagi, "III-V single structure CMOS by using ultrathin body InAs/GaSb-OI channels on Si," *Technology Digest – Symposium of VLSI*, 2014, pp. 34-35.

[123] M. Radosavljevic, T. Ashley, A. Andreev, S. D. Coomber, G. Dewey, M. T. Emeny, M. Fearn, D. G. Hayes, K. P. Hilton, M. K. Hudait, R. Jefferies, T. Martin, R. Pillarisetty, W. Rachmady, T. Rakshit, S. J. Smith, M. J. Uren, D. J. Wallis, P. J. Wilding, and R. Chau, "High-performance 40 nm gate length InSb p-channel compressively strained quantum well field effect transistors for low-power (V_{CC} = 0.5 V) logic applications," *Technical Digest – International Electron Devices Meeting*, 2008, pp. 727-730.

[124] K. Nishi, M. Yokoyama, H. Yokoyama, M. Takenaka, and S. Takagi, "Thin body GaSb p-MOSFETs on Si wafers fabricated by direct wafer bonding," in *Proceeding of Indium Phosphide Related Materials*, 2014, pp. 6-7.

[125] K. Nishi, M. Yokoyama, T. Hoshi, H. Sugiyama, M. Takenaka, and S. Takagi, "Operation of the GaSb p-channel metal-oxide-semiconductor field-effect transistors fabricated on {111}A surfaces," *Applied Physics Letters*, vol. **105**, no. 23, pp. 3503-3506, 2014.

[126] Z. Yuan, A. Kumar, C. -Y. Chen, A. Nainani, B. R. Bennett, J. B. Boos, and K. Saraswat, "Antimonide-based heterostructure p-channel MOSFETs with Ni-alloy source/drain,"

IEEE Transactions on Device Letters, vol. **34**, no. 11, pp. 1367-1369, 2013.

[127] S. Lee, C.-Y. Huang, D. C.-Elias, B. J. Thibeault, W. Mitchell, V. Chobpattana, S. Stemmer, A. C. Gossard, and M. J. W. Rodwell, "Highly scalable raised source/drain InAs quantum well MOSFETs exhibiting I_{ON} = 482 μA/μm at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 V," *Technology Digest – Symposium of VLSI*, 2012, pp. 177-178

[128] T.-W. Kim, R. J. W. Hill, C. D. Young, D. Veksler, L. Morassi, S. Oktyabrsky, J. Oh, C. Y. Kang, D.-H Kim, J. A. del Alamo, C. Hobbs, P. D. Kirsch, and R. Jammy, "InAs Quantum-Well MOSFET (L_g = 100 nm) with record high g_m, f_T and f_{max}," *Technology Digest – Symposium of VLSI*, 2012, pp. 179-180.

[129] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Sub-30nm InAs quantum-well MOSFETs with self-aligned metal contacts and sub-1 nm EOT HfO_2 insulator," *Technical Digest – International Electron Devices Meeting*, 2012, pp. 757-760.

[130] T.-W. Kim, D.-H Kim, D.-H. Koh, R. J. W. Hill, R. T. P. Lee, M. H. Wong, T. Cunningham, J. A. del Alamo, S. K. Banerjee, S. Oktyabrsky, A. Greene, Y. Ohsawa, Y. Trickett, G. Nakamura, Q. Li, K. M. Lau, C. Hobbs, P. D. Kirsch, and R. Jammy, "ETB-QW InAs MOSFET with scaled body for improved electrostatics," *Technical Digest – International Electron Devices Meeting*, 2012, pp. 765-768.

[131] M. Yokoyama, K. Nishi, S. Kim, H. Yokoyama, M. Takenaka, and S. Takagi, "Self-aligned Ni-GaSb source/drain junctions for GaSb p-channel metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters*, vol. **104**, no. 9, pp. 3509-3512, 2014.

[132] R. M. Sieg, J. A. Carlin, J. J. Boeckl, S. A. Ringel, M. T. Currie, S. M. Ting, T. A. Langdo, G. Taraschi, E. A. Fitzgerald, and B. M. Keyes, "High minority-carrier lifetimes

in GaAs grown on low-defect-density Ge/GeSi/Si substrates," *Applied Physics Letters*, vol. **73**, no. 21, pp. 3111-3113, 1998.

[133] G. Vanamu, A. K. Datyel, and S. H. Zaidi, " Epitaxial growth of high-quality Ge films on nanostructured silicon substrates," *Applied Physics Letters*, vol. **88**, no. 20, pp. 1909-1912, 2006.

[134] K. Hjort, "Transfer of InP epilayers by wafer bonding," *Journal of Crystal Growth*, vol. **268**, no. 3, pp. 346-358, 2004.

[135] P. Chen, Y. Jing, S. S. lau, D. Xu, L. Mawst, T. L. Alford, C. Paulson, and T. F. Kuech, "High crystalline-quality III-V layer transfer onto Si substrate," *Applied Physics Letters*, vol. **92**, no. 9, pp 2107-2110, 2008.

[136] H. Kroemer, "Polar on non-polar epitaxy", *Journal of Crystal Growth*, vol. 81, pp. 193-204, 1987.

[137] D. J. Chadi, "Stabilities of single-layer and bilayer steps on Si (001) surfaces", *Physics Review Letter*s, vol. 59, no. 15, 1987.

[138] K. Nishi, M. Yokoyama, H. Yokoyama, T. Hoshi, H. Sugiyama, M. Takenaka, and S. Takagi, "High hole mobility front-gate InAs/InGaSb-OI single structure CMOS on Si," *Technology Digest – Symposium of VLSI*, 2015, pp. 174-175.

[139] J. J. Gu, X. W. Wang, J. Shao, A. T. Neal, M. j. Manfra, R. G. Gordon, and P. D. Ye, "III-V gate-all-around nanowire MOSFET process technology: from 3D to 4D," *Technical Digest – International Electron Devices Meeting*, 2012, pp. 529-532.

[140] S. H. Huang. G. Balakrishnan, M. Mehta, A. Khoshakhlagh, L. R. Dawson, and D. L. Huffaker, " Epitaxial growth and formation of interfacial misfit array for tensile GaAs on GaSb," *Applied Physics Letters*, vol. **90**, no. 16, pp. 1902-1904, 2007.

[141] K. H. Tan, B. W. Jia, W. K. Loke, S. Wicaksono, and S. F. Yoon, "Formation of interfacial misfit dislocation in GaSb/GaAs heteroepitaxy via anion exchange process", *Journal of Crystal Growth*, vol. 427, pp. 80-86, 2015.

[142] Klimeck, "sp^3s^* and $sp^3d^5s^*$ tight-binding parameter sets for GaAs, AlAs, InAs, GaSb, AlSb, InSb, GaP,AlP, and InP for quantum dot simulations", *American Physical Society*, 2000.

[143] X. Zhang, H. Guo, X. Gong, Q. Zhou, H.-Y. Lin, Y.-R. Lin, C.-H. Ko, C. H. Wann, and Y.-C. Yeo, "$In_{0.7}Ga_{0.3}As$ channel n-MOSFETs with a novel self-aligned Ni-InGaAs contact formed using a salicide-like metallization process," in *proceedings of the VLSI Technology, Systems and Application* (*VLSI-TSA)*, *IEEE*, 2011, pp. 26-27.

[144] Ivana, J. Pan, Z. Zhang, X. Zhang, H. Guo, X. Gong, and Y.-C. Yeo, "Photoelectron spectroscopy study of band alignment at interface between Ni-InGaAs and $In_{0.53}Ga_{0.47}As$," *Applied Physics Letters*, vol. **99**, no. 1, pp. 2105-2107, 2011.

[145] X. Zhang, Ivana, H. Guo, X. Gong, Q. Zhou, and Y.-C. Yeo, "A self-aligned Ni-InGaAs contact technology for InGaAs channel n-MOSFETs," *Journal of the Electrochemical Society*, vol. **159**, no. 5, pp. 511-520, 2012.

[146] H. D. Trinh, G. Brammertz, E. Y. Chang, C. I. Kuo, C. Y. Lu, Y. C. Lin, H. Q. Nguyen, Y. Y. Wong, B. T. Tran, K. Kakushima, and H. Iwai, "Electrical Characterization of Al_2O_3/n-InAs metal-oxide-semiconductor capacitors with various surface treatments," *IEEE Electron Device Letters*, vol. **32**, no. 6, pp. 752-754, 2011.

[147] H. Luth, "Solid surfaces, interfaces and thin films," *New York: Springer-Verlag*, 2001.

[148] P. Tsipas and A. Dimolulas, "Modeling of negatively charged states at the Ge surface and interfaces," *Applied Physics Letters*, vol. **94**, no. 1, pp. 2114-2117, 2009.

[149] D. Kuzum, J. –H. Krishnamohan, H. –S. P. Wong, and K. Saraswat, "The effect of donor/acceptor nature of interface traps on Ge MOSFET characteristics," *IEEE Transactions on Electron Devices*, vol. **58**, no. 4, pp. 1015-1022, 2011.

[150] H. -S. P. Wong, "Beyond the conventional transistor," *IBM Journal of Research and Development*, vol. **46**, no. 2, pp. 133-168, 2002.

[151] A. C. Seabaugh and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," *Proceedings of the IEEE*, vol. **98**, no. 12, pp. 2095-2110, 2010.

[152] D. E. Nikonov and I. A. Young, "Overview of beyond-CMOS devices and a uniform methodology for their benchmarking," *Proceedings of the IEEE*, vol. 101, no. 12, pp. 2498-2533, 2013

[153] S. K. Banerjee, L. F. Register, E. Tutuc, D. Basu, S. Kim, and A. H. MacDonald, "Graphene for CMOS and Beyond CMOS applications," *Proceeding of IEEE*, vol. **98**, no. 12, pp. 2032-2046, 2010.

[154] S. Fujita, K. Nomura, K. Abe, and T. H. Lee, "3-D nanoarchitectures with carbon nanotube mechanical switches for future on-chip network beyond CMOS architecture," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. **54**, no. 11, pp. 2472-2479, 2007.

[155] J. J. Gu, Y. Q. Liu, T. Q. Wu, R. Colby, R. G. Gordon, and P. D. Ye, "First experimental demonstration of gate-all-around III-V MOSFETs by top down approach," *Technical Digest – International Electron Devices Meeting*, 2011, pp. 769-772.

[156] K. Tachi, S. Barraud, K. Kakushima, H. Iwai, S. Cristoloveanu, T. Ernst, "Comparison of low-temperature electrical characteristics of gate-all-around nanowire FETs, FinFETs

and fully-depleted SOI FETs," *Microelectronics Reliability*, vol. **51**, no. 5, pp. 885-888, 2011.

[157] K. D. Buddharaju, N. Singh, S. C. Rustagi, S. H. G. Teo, L. Y. Wong, L. J. Tang, C. H. Tung, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "Gate-all-around Si-nanowire CMOS inverter logic fabricated using top-down approach," *Solid-State Electronics*, vol. **52**, no. 9, pp. 1312-1317, 2008.

[158] T. -Y. Liow, K. -M. Tan, R. T. P. Lee, M. Zhu, B. L. -H. Tan, Balasubramanian, and Y. -C. Yeo, "Germanium source and drain stressors for ultrathin-body and nanowire field-effect transistors," *IEEE Electron Device Letters*, vol. **29**, no. 7, pp. 808-810, 2008.

[159] Y. Song, H. Zhou, Q. Xu, J. Niu, J. Yan, H. Zhao, and H. Zhong, "High-performance silicon nanowire gate-all-around nMOSFETs fabricated on bulk substrate using CMOS-compatible process," *IEEE Electron Device Letters*, vol. **31**, no. 12, pp. 1377-1379, 2010.

[160] P. D. Ye, "III-V MOS technology: from planar to 3D and 4D," *25th International Conference on Indium Phosphide and Related Materials*, 2013, pp. 1-2.

[161] H. C. Chin, X. Gong, L. Wang, H. K. Lee, L. Shi, and Y. -C. Yeo, "III-V multiple-gate field-effect-transistors with high-mobility $In_{0.7}Ga_{0.3}As$ Channel and epi-controlled retrograde-doped fin," *IEEE Electron Device Letters*, vol. **32**, no. 2, pp. 146-148, 2011.

[162] S. Bangsaruntip, G. M. Cohen, A. Majumdar, Y. Zhang, S. U. Engelmann, N. C. M. Fuller, L. M. Gignac, S. Mittal, J. S. Newbury, M. Guillorn, T. Barwicz, L. Sekaric, M. M. Frank, and J. W. Sleight, "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," *Technical Digest – International Electron Devices Meeting*, 2009, pp. 297-300.

[163] T. Numata, M. Saitoh, Y. Nakabayashi, K. Ota, and K. Uchida, "Source/drain and gate engineering on Si nanowire transistors with reduced parasitic resistance and strained Silicon channel," *10th IEEE Intrenational Conference on Solid-State and Integrated Circuit Technology*, 2010, pp. 37-40.

[164] D. G. -Gordon, H. Shtrikman, D. Mahalu, D. A. -Magder, U. Meirav, and M. A. Kastner, "Kondo effect in a single-electron transistor," *Nature*, vol. **391**, no. 6663, pp. 156-159, 1998.

[165] J. Park, A. N. Pasupathy, J. I. Goldsmith, C. Chang, Y. Yaish, J. R. Petta, M. Rinkoski, J. P. Sethna, H. D. Abruna, P. L. McEuen, an D. C. Ralph, "Coulomb blockade and the Kondo effect in single-atom transistor," *Nature*, vol. **417**, no. 6890, pp. 722-725, 2002.

[166] K. K. Likharev, "Single-electron devices and their applications," *Proceedings of the IEEE*, vol. 87, no. 4, pp. 606-632, 1999.

[167] D. K. Klein, R. Roth, A. K. L. Lim, A. P. Alivisators, and P. L. McEuen, "A single-electron transistor made from a Cadmium Selenide nanocrystal," *Nature*, vol. **389**, no. 6652, pp. 699-701, 1997.

[168] H. W. Ch. Postma, T. Teepen, Z. Yao, M. Grifoni, C. Dekker, "Carbon nanotube single-electron transistors at room temperature," *Science*, vol. **293**, no. 6527, pp. 76-79, 2001.

[169] K. Matsumoto, M. Ishii, K. Segawa, and Y. Oka, "Room temperature operation of a single electron transistor made by the scanning tunneling microscope nanooxidation process for the TiO_x/Ti system," *Applied Physics Letters*, vol. **68**, no. 1, pp. 34-36, 1996.

[170] C. W. Wilmsen, "Physics and chemistry of III-V compound semiconductor interfaces", *Plenum* Press, New York, 1985.

[171] S. Pearton, "Handbook of advanced electronic and photonic materials and devices," *Academic Press*, 2001, pp. 191-190.

[172] N. J. Kadhim, S. H. Laurie, and D. Mukherjee, "Chemical etching of group III-V semiconductor," *Journal of Chemical Education*, vol. **75**, no. 7, pp. 840-843, 1998.

[173] M. C. Lavine, H. C. Gatos, and M. C. Finn, "Characteristics of the {111} surfaces of the III-V intermetallic compounds," *Journal of Electrochemistry Society*, vol. **108**, no. 10, pp. 974-980, 1961.

[174] H. H. Goossens and W. P, Gomes, "(Photo)electrochemistry suitable tool for investigating wet etching processes on III-V semiconductor*," Electrochimica Acta*, vol. **37**, no. 5,. Pp. 811-826, 1992.

[175] G. Wulff, "Zeitschrift für Kristallographie," *Crystalline Materials*, vol. **34**, no. 1, pp. 449-530, 1901.

[176] N. Miyata, H. Ishii, Y. Urabe. T. Itatani, T. Yasuda. H. Yamada, N. Fukuhara, M. Hata, M. Deura, M. Sugiyama, M. Takenaka, and S. Takagi, "Origin of electron mobility enhancement in (111)-oriented InGaAs channel metal-insulator-semiconductor field-effect-transistors," *Microelectronic Engineering*, vol. **88**, no. 12, pp. 3459-3461, 2011.

[177] H. Ishii, N. Miyata, Y. Urabe, T. Itatani, T. Yasuda, H. Yamada, N. Fukuhara, M. Hata, M. Deura, M. Sugiyama, M. Takenaka, and S. Takagi, "High Electron Mobility Metal-Insulator-Semiconductor Field-Effect Transistors Fabricated on (111)-oriented InGaAs Channels," *Applied Physics Express*, vol. **2**, no. 12, pp. 1101-1104, 2009.

[178] X. Zhang, H. Guo, X. Gong, Q. Zhou, Y.-R. Lin, H.-Y. Lin, C.-H. Ko, C. H. Wann, and Y.-C. Yeo, "$In_{0.7}Ga_{0.3}As$ channel n-MOSFET with self-aligned Ni-InGaAs source and drain," *Electrochemical Solid-State Letters*, vol. **14**, no. 2, pp. 60-62, 2011.

[179] X. Zhang, H. Guo, H.-Y. Lin, Ivana, X. Gong, Q. Zhou, Y.-R. Lin, C.-H. Ko, C. H. Wann, and Y.-C. Yeo, "Reduction of off-state leakage current in $In_{0.7}Ga_{0.3}As$ channel n-MOSFETs with self-aligned Ni-InGaAs contact metallization," *Electrochemical Solid-State Letters*, vol. **14**, no. 5, pp. 212-214, 2011.

[180] X. Zhang, H. Guo, X. Gong, Q. Zhou, H.-Y. Lin, Y.-R. Lin, C.-H. Ko, C. H. Wann, and Y.-C. Yeo, "$In_{0.7}Ga_{0.3}As$ channel n-MOSFETs with a novel self-aligned Ni-InGaAs contact formed using a salicide-like metallization process," in *Proceedings of the VLSI Technology, Systems and Application* (*VLSI-TSA)*, *IEEE*, 2011, pp. 26-27.

[181] Ivana, J. Pan, Z. Zhang, X. Zhang, H. Guo, X. Gong, and Y.-C. Yeo, "Photoelectron spectroscopy study of band alignment at interface between Ni-InGaAs and $In_{0.53}Ga_{0.47}As$," *Applied Physics Letters*, vol. **99**, no. 1, pp. 2105-2107, 2011.

[182] X. Zhang, Ivana, H. Guo, X. Gong, Q. Zhou, and Y.-C. Yeo, "A self-aligned Ni-InGaAs contact technology for InGaAs channel n-MOSFETs," *Journal of the Electrochemical Society*, vol. **159**, no. 5, pp. 511-520, 2012.

[183] O. Kumar and M. Kaur, "Single electron transistor: application and problem," *International Journal of VLSI Design and Communication Systems*, vol. **1**, no. 4, pp. 24-29, 2010.

[184] V. Mittal, "Basic introduction to single electron transistor*," International Journal for Research in Applied Science and Engineering Technology*, vol. **1**, no. 1, pp. 9-13, 2013.

[185] K. H. Goh, Y. Guo, X. Gong, G.-C. Liang, and Y.-C. Yeo, "Near ballistic sub-7 nm $In_{0.53}Ga_{0.47}As$ junctionless FET featuring 1 nm extremely-thin channel and raised S/D structure," *IEEE International Electron Device Meeting 2013*, Washington, DC USA, Dec. 9 - 11, 2013.

[186] K. H. Goh, Y. Cheng, K. L. Low, E. Y. J. Kong, C.-K. Chia, E.-H. Toh, and Y.-C. Yeo, "Physical model for gallium arsenide growth on germanium fins with different orientations formed on 10° offcut germanium-on-insulator substrate," *J. Applied Physics*, vol. 113, no. 4, 044103, Jan. 2013.

[187] K. H. Goh, Y. Cheng, K. L. Low, E. Y. J. Kong, C.-K. Chia, E.-H. Toh, and Y.-C. Yeo, "Selective growth of gallium arsenide on germanium fins with different orientations formed on 10° offcut germanium-on-insulator substrate," *International Conference on Solid-State Devices and Materials*, Kyoto, Japan, Sep. 25 - 27, 2012.

[188] K. H. Goh, K. H. Tan, S. Yadav, A. Kumar, S. -F. Yoon, G. Liang, X. Gong, and Y. -C. Yeo, "Gate-all-around CMOS (InAs n-FET and GaSb p-FET) based on vertically stcaked naowires on a Si platform, enabled by extremely-thin buffer layer technology and common gate stack and contact modules," (submitted to *IEEE International Electron Device Meeting 2015*)

[189] K. H. Goh and Y.-C. Yeo, "Novel short-channel $In_{0.53}Ga_{0.47}As$ junctionless nanowire nFET with raised S/D structure: An ultimately scaled 1-D transistor architecture," *2014 Silicon Nanoelectronics Workshop* (*SNW*), Honolulu HI, USA, June 8-9, 2014.

Appendix

A1 *Layout for the Fabrication of JLFETs*

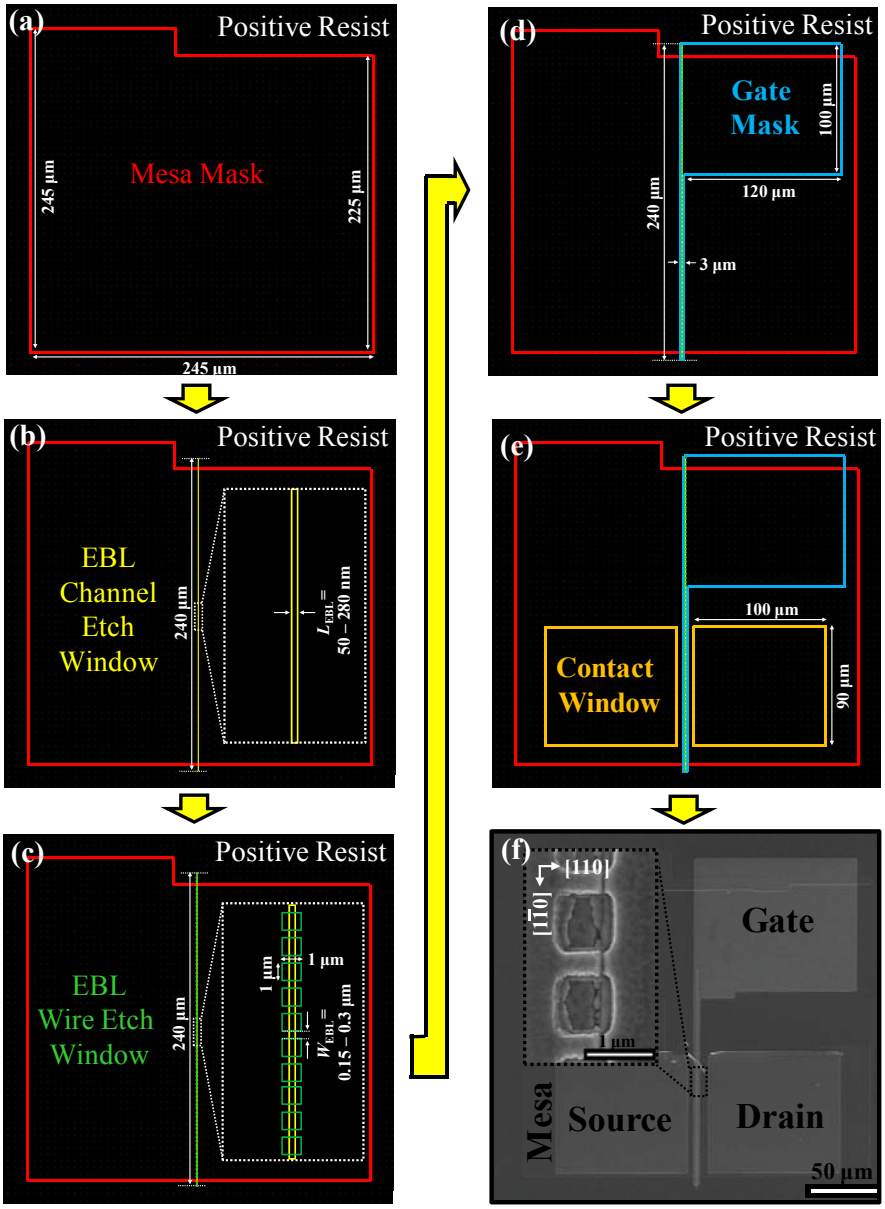


Fig. A1 Layout used for the fabrication of JLFET during (a) mesa formation, (b) wire formation, (c) channel formation, (d) gate formation, and (e) contact formation. (f) Top-view SEM image of a completed JLFET device. Inset shows the zoomed in SEM view of the channel region of the JLFET device

A2 *Layout for the Fabrication of Vertically Stacked NWs CMOS on Si*

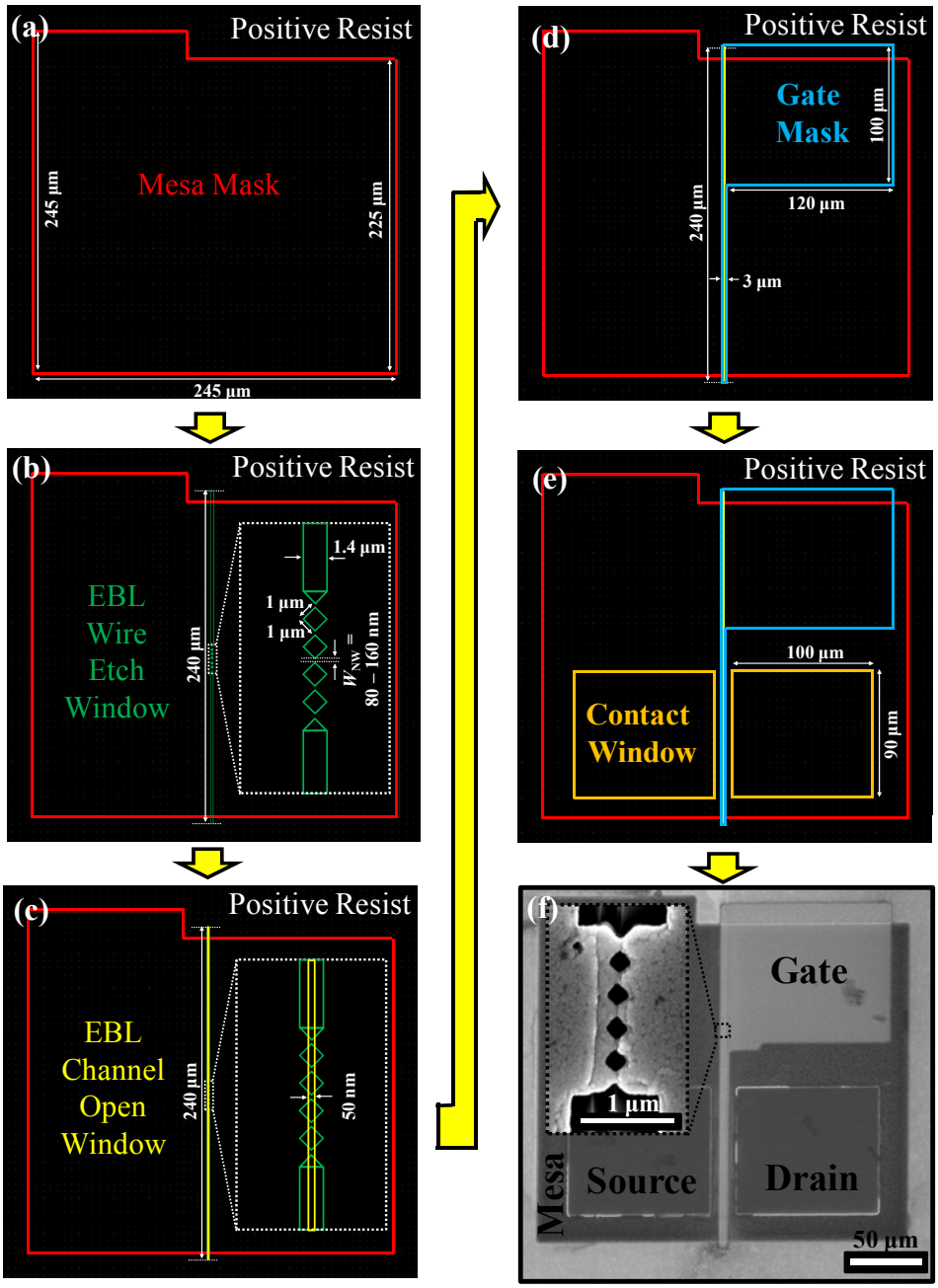


Fig. A2 Layout used for the fabrication of vertically stacked NWs CMOS on silicon during (a) mesa formation, (b) wire formation, (c) channel formation, (d) gate formation, and (e) contact formation. (f) Top-view SEM image of a completed NWFET device. Inset shows the zoomed in SEM view of the channel region of the vertically stacked NWs CMOS on silicon device.

A3 *Layout for the Fabrication of NWFETs with Tapered S/D Structure*

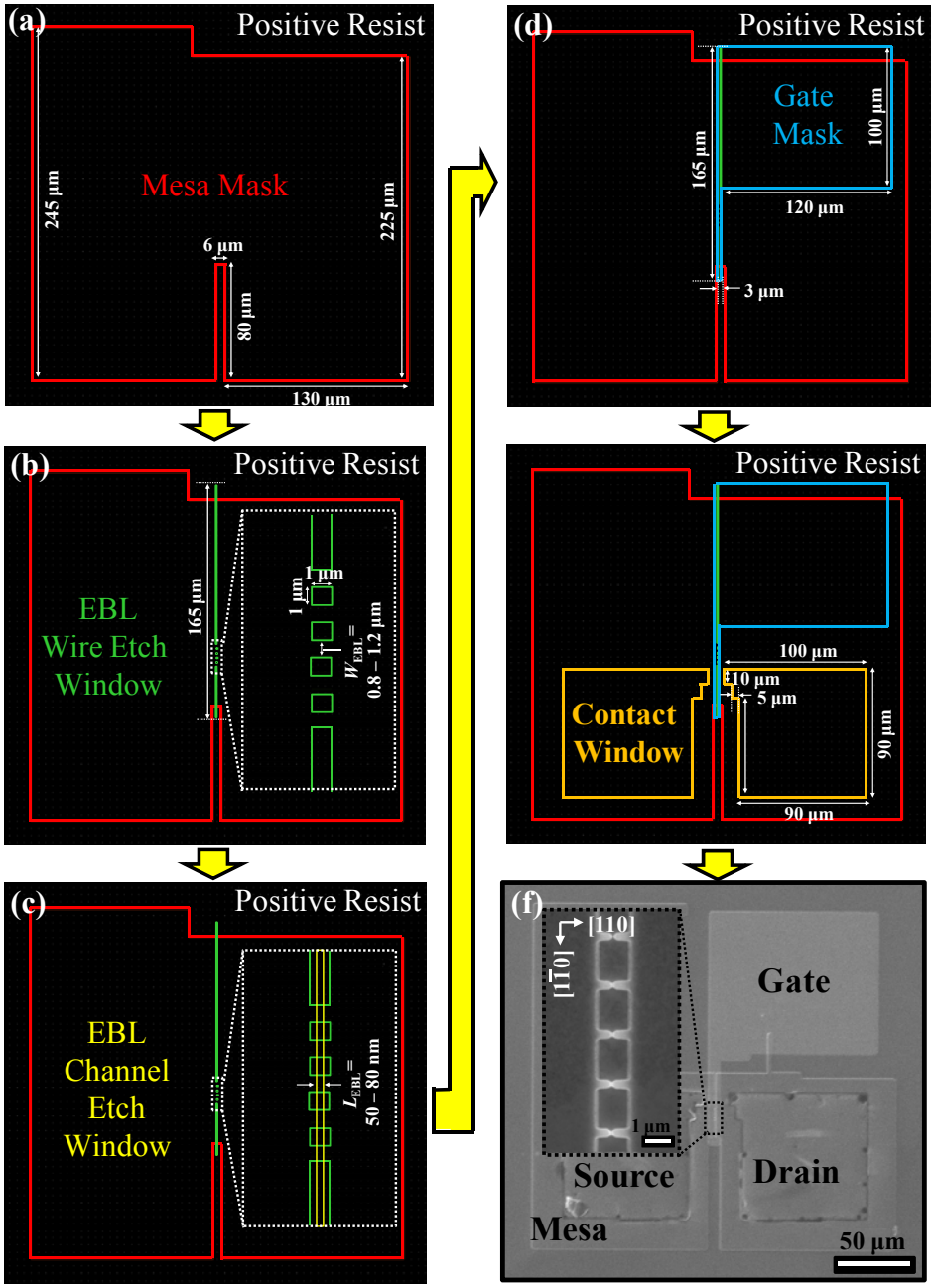


Fig. A3 Layout used for the fabrication of NWFET with tapered S/D structure during (a) mesa formation, (b) wire formation, (c) channel formation, (d) gate formation, and (e) contact formation. (f) Top-view SEM image of a completed NWFET device. Inset shows the zoomed in SEM view of the channel region of the NWFET device.

List of Publications

Journal Publications

[1] **K. H. Goh**, Y. Cheng, K. L. Low, E. Y. J. Kong, C.-K. Chia, E.-H. Toh, and Y.-C. Yeo, "Physical model for gallium arsenide growth on germanium fins with different orientations formed on 10° offcut germanium-on-insulator substrate," *Journal of Applied Physics*, vol. **113**, no. 4, pp. 4103-4113, 2013.

Conference Publications

[2] **K. H. Goh**, Y. Guo, X. Gong, G.-C. Liang, and Y.-C. Yeo, "Near ballistic sub-7 nm $In_{0.53}Ga_{0.47}As$ junctionless FET featuring 1 nm extremely-thin channel and raised S/D structure," *IEEE International Electron Device Meeting 2013*, 2013.

[3] **K. H. Goh**, Y. Cheng, K. L. Low, E. Y. J. Kong, C.-K. Chia, E.-H. Toh, and Y.-C. Yeo, "Selective growth of gallium arsenide on germanium fins with different orientations formed on 10° offcut germanium-on-insulator substrate," *International Conference on Solid-State Devices and Materials*, 2012.

[4] **K. H. Goh**, K. H. Tan, S. Yadav, A. Kumar, S. -F. Yoon, G. Liang, X. Gong, and Y. -C. Yeo, "Gate-all-around CMOS (InAs n-FET and GaSb p-FET) based on vertically stcaked naowires on a Si platform, enabled by extremely-thin buffer layer technology and common gate stack and contact modules," (submitted to *IEEE International Electron Device Meeting 2015*).

[5] **K. H. Goh** and Y.-C. Yeo, "Novel short-channel $In_{0.53}Ga_{0.47}As$ junctionless nanowire nFET with raised S/D structure: An ultimately scaled 1-D transistor architecture," *2014 Silicon Nanoelectronics Workshop* (*SNW*), 2014.

List of Co-Authored Publications

Journal Publications

[6] K. L. Low, C. Zhan, G. Han, Y. Yang, **K.-H. Goh**, P. Guo, E.-H. Toh, and Y.-C. Yeo, "Device physics and design of a L-shaped Germanium source tunneling transistor," *Japanese Journal of Applied Physics*, vol. **51**, no. 2, pp. 02BC04:1-6, 2012.

Conference Publications

[7] K. L. Low, C. Zhan, G. Han, Y. Yang, **K. H. Goh**, P. Guo, E.-H. Toh, and Y.-C. Yeo, "Tunnel field-effect transistor with L-shaped germanium source: Device physics and design," *Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials*, 2011, pp. 849 - 850.

[8] G. Han, Y. Yang, P. Guo, C. Zhan, K. L. Low, **K. H. Goh**, B. Liu, E.-H. Toh, and Y.-C. Yeo, "PBTI characteristics of n-channel tunneling feld effect transistor with HfO_2 gate dielectric: New insights and physical model," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), 2012.

[9] X. Gong, Z. Zhu, E. Kong, R. Cheng, S. Subramanian, **K. H. Goh**, and Y.-C. Yeo, "Ultra-thin-body $In_{0.7}Ga_{0.3}As$ on nothing N-MOSFET with Pd-InGaAs S/D contacts enabled by a new self-aligned cavity formation technology," *International Symposium on VLSI Technology, Systems and Applications* (*VLSI-TSA*), 2012.

[10] R. Cheng, X. Gong, P. Guo, F. Bai, Y. Yang, B. Liu, **K. H. Goh**, S. Su, G. Zhang, C. Xue, B. Cheng, G. Han, and Y.-C. Yeo, "Top-down GeSn nanowire formation using F-

based dry etch and H_2O_2-based wet etch," *43rd Semiconductor Interface Specialist Conference*, 2012.

[11] G. Han, X. Gong, F. Bai, R. Cheng, P. Guo, **K. H. Goh**, S. Su, G. Zhang, C. Xue, B. Cheng, and Y.-C. Yeo, "(111)-oriented strained GeSn channel pMOSFET with low temperature Si_2H_6 surface passivation," *43rd Semiconductor Interface Specialist Conference*, 2012.

[12] X. Gong, G. Han, S. Su, R. Cheng, P. Guo, F. Bai, Y. Yang, Q. Zhou, **K. H. Goh**, G. Zhang, C. Xue, B. Cheng, and Y.-C. Yeo, "Uniaxially strained germanium-tin (GeSn) gate-all-around nanowire PFETs enabled by a novel top-down nanowire formation technology," *Symposium on VLSI Technology,* 2013, pp. 34 - 35.